VV6501

VGA CMOS Color Image Sensor

Features

- **640 x 480 VGA resolution**
- **1/4 inch format lens compatible**
- **On board 10 bit ADC**
- **On board voltage regulators**
- **Automatic dark calibration**
- **On board audio amplifier**
- **I^2C interface**
- **Low power suspend mode**
- **4 or 5 wire nibble output**
- **Framegrabber signals: QCK and FST**

Description

This image sensor based on STMicroelectronics CMOS technology is Bayer colorised.

The sensor provides a raw digital video output which also contains embedded codes to facilitate external synchronisation.

The sensor interfaces to a range of STMicroelectronics companion processors for applications such as USB webcams and digital stills cameras.

An I^2C interface allows an external processor to configure the device and control exposure and gain settings.

A low-power pin-driven suspend mode simplifies USB-based designs.

On board voltage regulators operate from a 5V USB supply and generate 3V3 and 1V8 power supplies for external processors.

Technical Specifications

Image Size	640 x 480 (VGA)	
Pixel size	5.6 µm x 5.6 µm	
Array size	3.6 mm x 2.7 mm	
Analogue gain	x1 to x16	
Sensitivity (typ.)	2.05 V/lux-sec	
Maximum frame rate	30 fps (with 24MHz clock)	
Supply voltage	5V (USB)	
	3V3 direct drive	
Power consumption	Active (30fps)	< 30 mA
	Suspend	< 100 µA
Operating temperature	0^oC - 40^oC	
Package type	36 pin CLCC	

Ordering Details

Part Number	Description
VV6501C001	36pin CLCC, colorised sensor

Table of Contents

1 Overview

1.1 Sensor overview

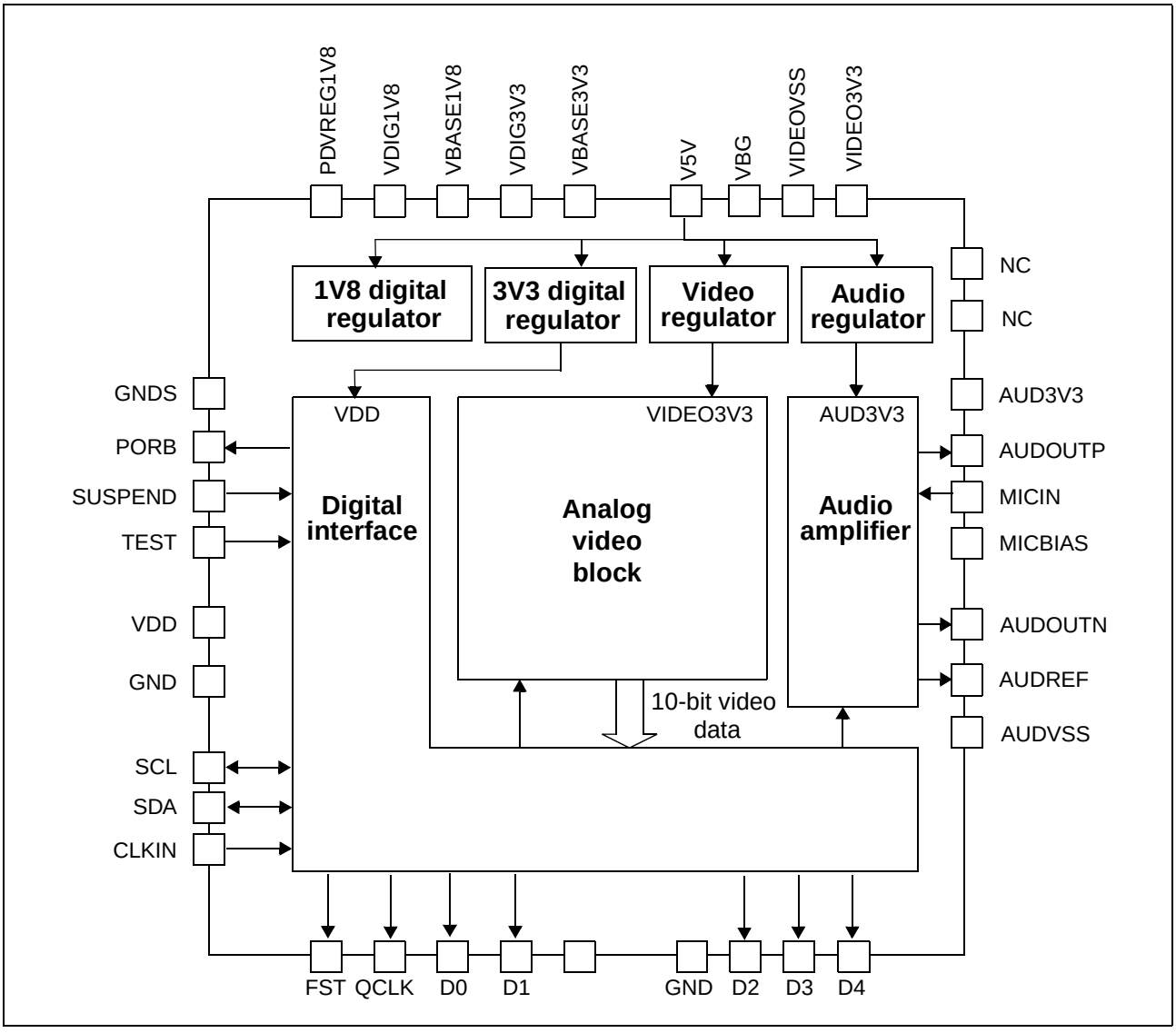
The VV6501 VGA image sensor produces raw digital video data at up to 30 frames per second. The image data is digitised using an internal 10-bit column ADC. The resulting 10-bit output data includes embedded codes for synchronization. The data is formatted as 5-bit nibbles. A separate data qualification clock (qck) and frame start (fst) signals are also provided.

The sensor is fully configurable using an I^2C interface.

The sensor also contains an audio low-noise preamplifier for use with an external microphone.

The sensor is optimized for USB applications and contains voltage regulators which drive external pass transistors to produce 3V3 and 1V8 supplies. These supplies may be used by external processors. A dedicated SUSPEND input pin may be used to force the device into a low power state while maintaining the device configuration. A power-on reset signal (PORB) may be used to reset external devices.

Figure 1: VV6501 block diagram



1.2 Typical application

1.2.1 USB webcam

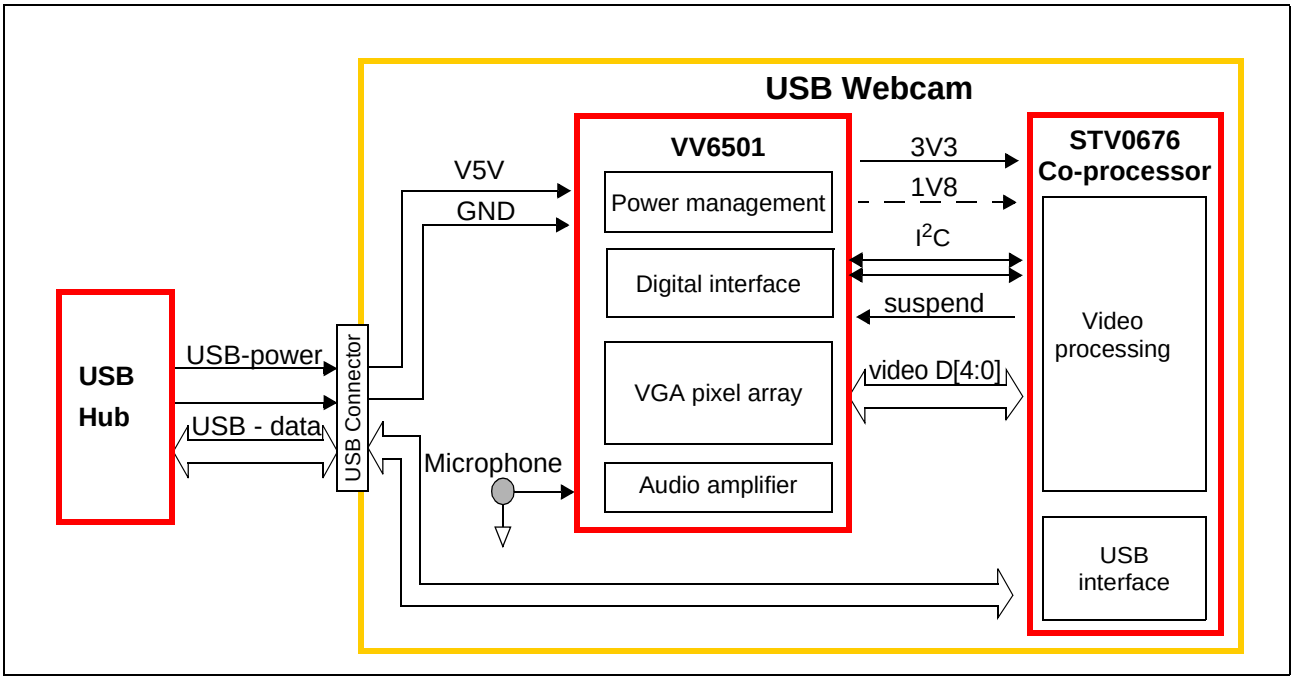
This sensor may be used in conjunction with the STMicroelectronics STV0676 co-processor to produce a low cost USB webcam.

In this application the co-processor supplies the sensor clock and uses the embedded control sequences to synchronise with the frame and line level timings. It then performs the colour processing on the raw image data from the sensor before supplying the final image data to the host using the USB interface.

The voltage regulators on-board the sensor are used to control external bipolar transistors to derive the supplies for the sensor and co-processor from the 5V USB supply. This approach eliminates the requirement for more costly external voltage regulation circuitry.

Figure 2 below illustrates a typical system using VV6501.

Figure 2: USB camera system using STV0676

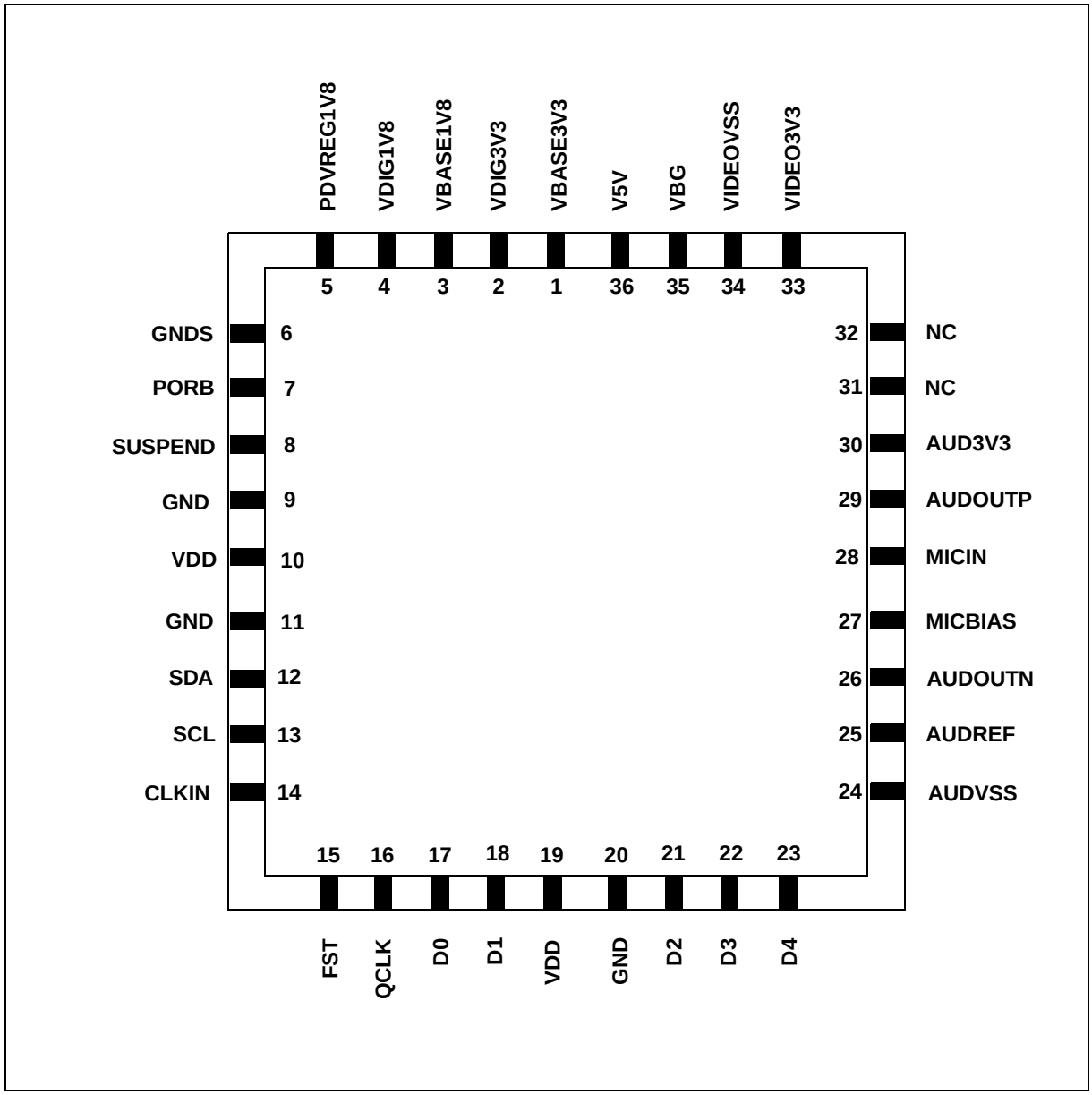


The input USB supply is 5 V. The 3V3 digital regulator generates the supply for the sensor digital part and the co-processor IOs. The 1V8 regulator generates the core supply for the co-processor.

2 Device Pinout

2.1 Pin position

Figure 3: Pin position



2.2 Pin description

Table 1: Pin description

Pin Number	Pin Name	Pin Type	Description
Digital regulators			
1	VBASE3V3	PWR	3.3 V digital regulator (connect to external PNP base)
2	VDIG3V3	PWR	3.3 V digital regulator (connect to external PNP collector)
3	VBASE1V8	PWR	1.8 V digital regulator (connect to external PNP base)
4	VDIG1V8	PWR	1.8 V digital regulator (connect to external PNP collector)
Digital inputs/outputs			
5	PDVREG1V8	PWR	1.8 V reg power down signal 1 - Regulator powered down 0 - Regulator powered up
6	GNDS	PWR	Connect to GND
7	PORB	O	Power on reset signal (active low)
8	SUSPEND	I	Sensor suspend input signal (active high) with Schmitt buffer
9	TEST	I	Input pin with Schmitt buffer. Connect to GND
10	VDD	PWR	Digital IO supply 3.3 V
11	GND	PWR	Digital ground
12	SDA	IO	Bidirectional I^2C pin
13	SCL	IO	Bidirectional I^2C pin. I^2C clock line
14	CLKIN	I	Input clock pin with Schmitt buffer
15	FST	O	FST signal (active high). 2 mA output pad
16	QCLK	O	Sensor data qualifying clock. 4 mA output pad
17	D0	O	D0 signal (data bus, bit 0). 4 mA output pad
18	D1	O	D1 signal (data bus, bit 1). 4 mA output pad
19	VDD	PWR	Digital IO supply 3.3V
20	GND	PWR	Digital IO/core source ground
21	D2	O	D2 signal (data bus, bit 2). 4 mA output pad
22	D3	O	D3 signal (data bus, bit 3). 4 mA output pad
23	D4	O	D4 signal (data bus, bit 4). 4 mA output pad

Table 1: Pin description

Pin Number	Pin Name	Pin Type	Description
Audio amplifier			
24	AUDVSS	PWR	Audio ground
25	AUDREF	PWR	Audio reference voltage (requires external decoupling capacitor)
26	AUDOUTN	O	Audio negative output
27	MICBIAS	PWR	Audio microphone bias voltage
28	MICIN	I	Audio microphone input signal
29	AUDOUTP	O	Audio positive output
30	AUD3V3	PWR	3.3 V audio analogue supply (requires external decoupling capacitor)
Video regulator			
33	VIDEO3V3	PWR	Analogue video 3.3 V
34	VIDEOVSS	PWR	Analogue video ground
35	VBG	PWR	5 V BandGap voltage (requires external decoupling capacitor)
36	V5V	PWR	USB power supply (4 - 5.5 V)
Not connected			
31,32	-	-	Not connected

3 Functional Description

The first three sections of this chapter detail the main blocks in the device:

- Video
- Audio
- Power management

The final section describes the device level operating modes including suspend.

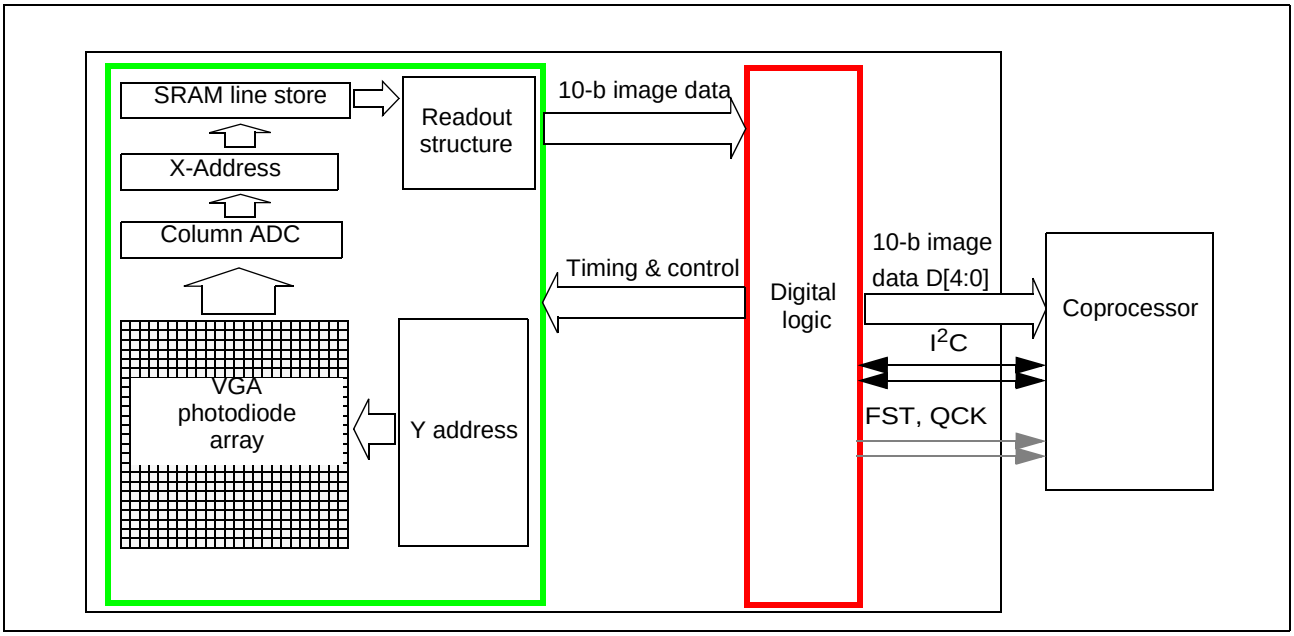
3.1 Video block

3.1.1 Overview

The analog core of the video block contains a VGA sized pixel array. The integration time and access for a row of pixels is controlled by the Y-address block. The row of pixels being read is converted using a 10-bit in-column ADC. The digitised data is readout into the digital block for formatting. The 10-b data is transferred to the co-processor over a 5-wire digital bus as two 5-b nibbles.

The exposure or integration time for the pixel array is calculated by the external co-processor and delivered to the sensor using the I2C interface.

Figure 4: Overview of video block

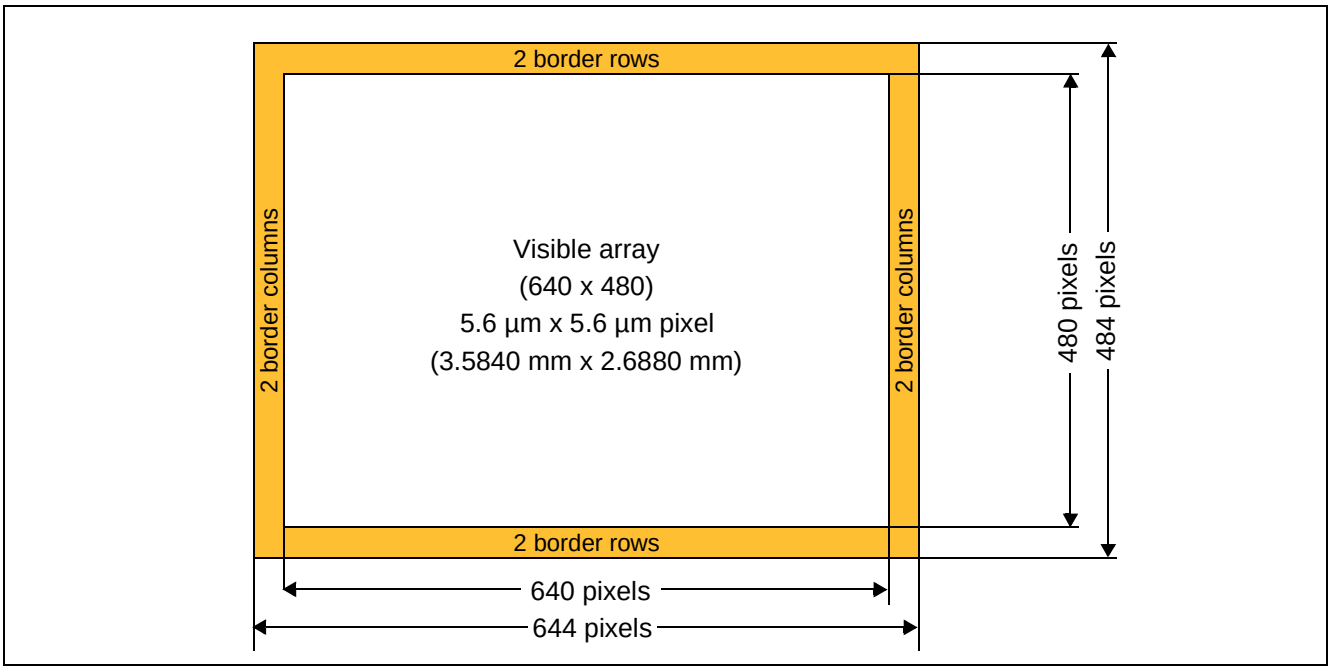


Data synchronization can be achieved either by using the embedded codes within the data stream or by making use of the dedicated FST and QCK pins.

3.1.2 Imaging array

The physical pixel array is 656 x 496 pixels. The pixel size is 5.6 µm by 5.6 µm.

Figure 5: Pixel array



The additional border columns and rows are included to enable complete color reconstruction of the final 640 by 480 sized array.

Microlens

Microlenses placed above the visible pixels improve light gathering capability hence improving sensitivity.

3.1.3 Sensor data overview

Sensor data is output on a 5-wire bus. As well as pixel data there are embedded codes at the start and end of every video line. These codes are always preceded by an escape sequence which is guaranteed not to appear in the video data itself.

Table 2: Video data values

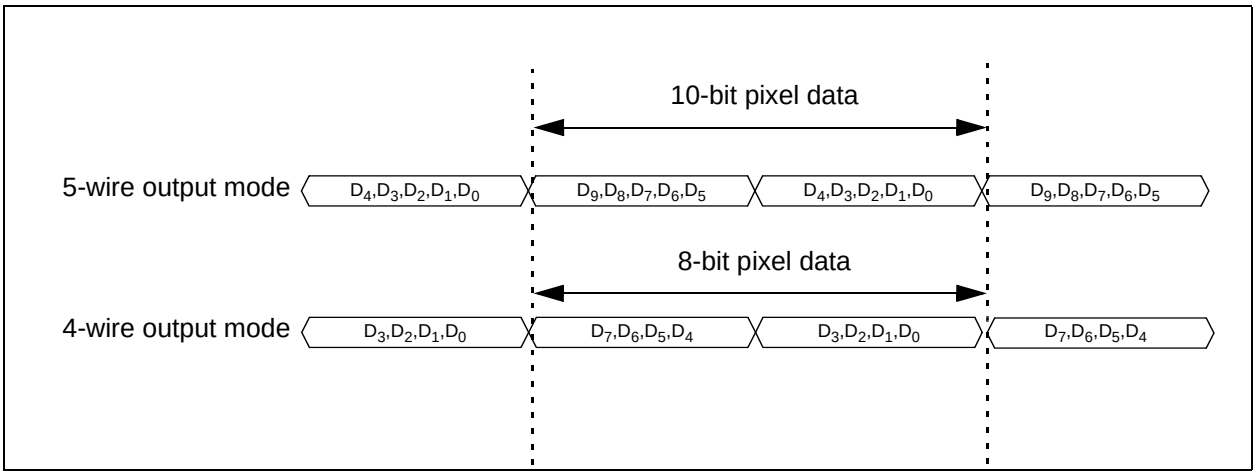
Read-out order	Progressive scan (non-interlaced)	
Form of encoding	Uniformly quantized, PCM, 8/10 bits per sample	
	8 bit mode	**10 bit mode**
Video pixel range	1 to 254	1 to 1022
Black level value	16	64
Escape sequence	FF, FF, 00	3FC, 3FC, 00

3.1.4 Digital data bus: D[4:0]

Sensor data may be either 8 or 10 bits per pixel and is transmitted as follows:

- **10-bit data:** A pair of 5-bit nibbles, most significant nibble first, on 5 wires.
- **8-bit data:** A pair of 4-bit nibbles, most significant nibble first, on 4 wires.

Figure 6: Digital data output modes



In 5-wire mode, the embedded control codes occupy only the most significant 8-bits, the least significant 2-bits are always zero.

Output tri-state using SIF

Register 23 bit[5] can be used to tri-state all 5 data lines, QCK and FST.

Output pad drive strength

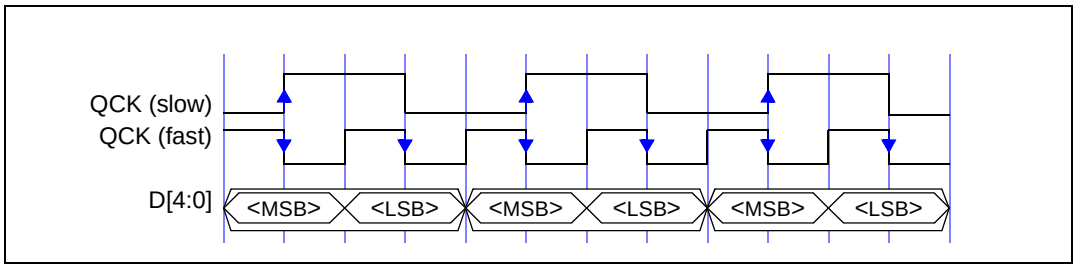
The data and QCK output pads are tri-stateable with 4 mA drive.

3.1.5 Data qualification clock (QCK)

A data qualification clock (QCK) is available and complements the embedded control sequences. This clock runs continuously when enabled and consists of:

- **Fast QCK**: the falling edge of the clock qualifies every 5 or 4-bit data blocks that constitute a pixel value.
- **Slow QCK**: the rising edge qualifies 1st, 3rd, 5th, etc. blocks of data that constitute a pixel value while the falling edge qualifies the 2nd, 4th, 6th etc. blocks of data. For example in 4-wire mode, the rising edge of the clock qualifies the most significant nibbles while the falling edge of the clock qualifies the least significant nibbles.

Figure 7: QCK modes

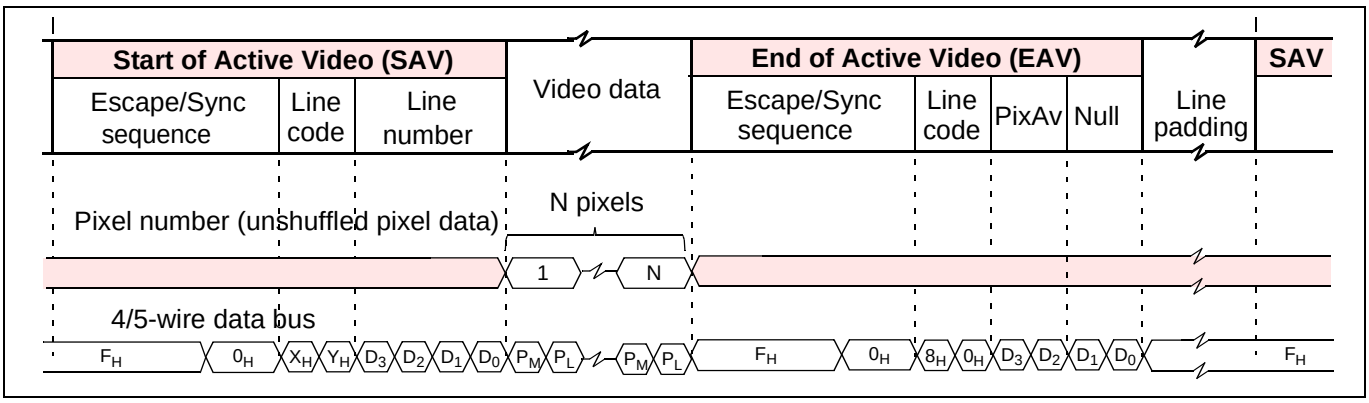


3.1.6 Line formats

Each line of data from the sensor starts with an escape sequence followed by a line code that identifies the line type. The line code is then followed by two bytes that contain a coded line number.

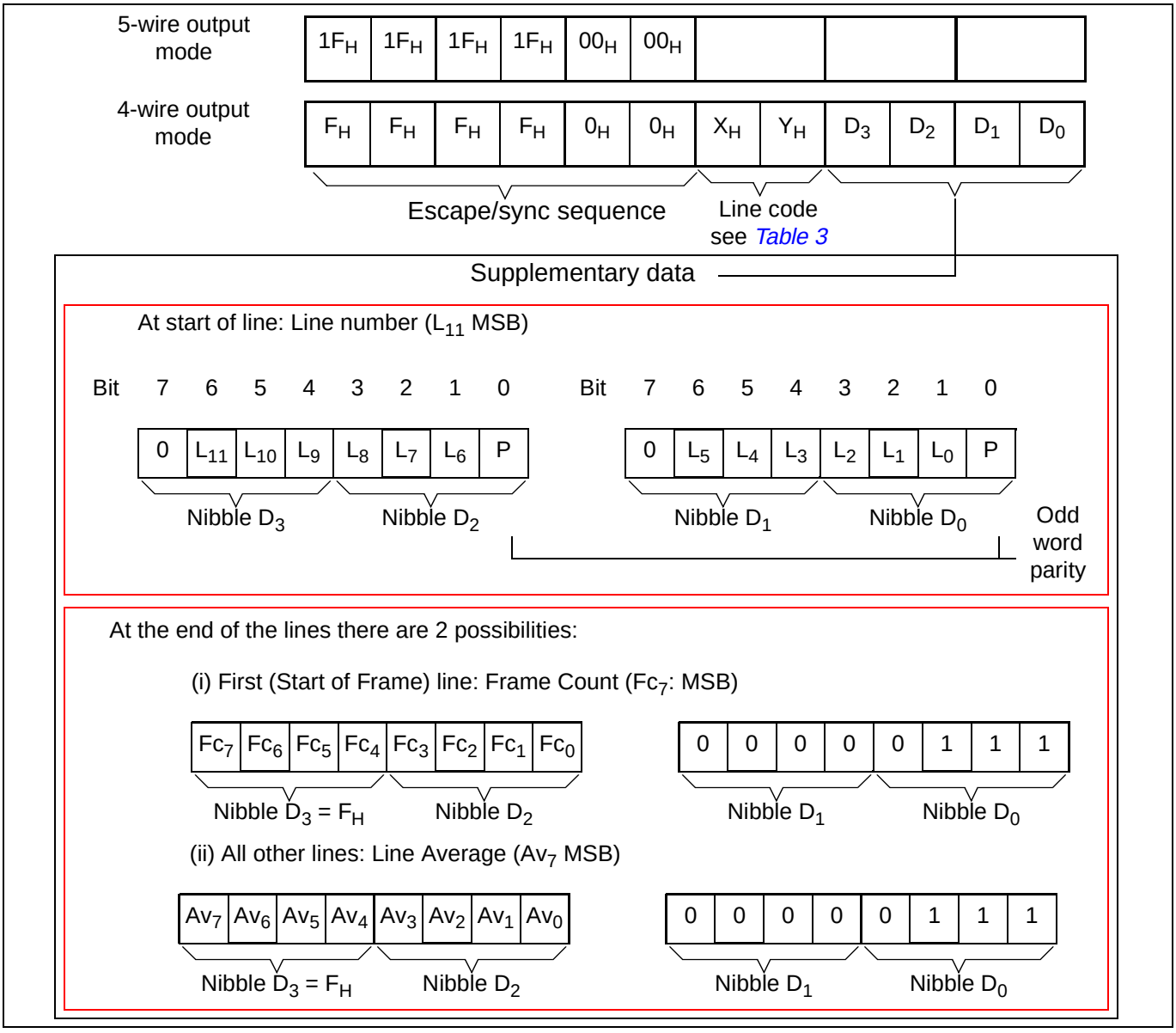
Each line is terminated with an end-of-line code followed by a line average. The one exception to this is the first line in the frame where the end of line code is followed by a frame count.

Figure 8: Line data format



The line code formats are detailed in *Figure 9*.

Figure 9: Line code format



The line code absolute value depends on whether 5-wire or 4-wire output mode has been selected, as shown in *Table 3*.

Table 3: Line codes

Line code	5-b Nibbles	4-b Nibbles
Line codes at beginning of line		
Start of Frame	$31C_H$ (796_{10})	$C7_H$ (199_{10})
Blank Line (BL)	274_H (628_{10})	$9D_H$ (157_{10})
Black or Dark line (BK)	$2AC_H$ (684_{10})	AB_H (171_{10})
Visible Line (VL)	$2D8_H$ (728_{10})	$B6_H$ (182_{10})
Last line in Frame	368_H (872_{10})	DA_H (218_{10})
Line Code at end of line		
End of Line	200_H (512_{10})	80_H (128_{10})

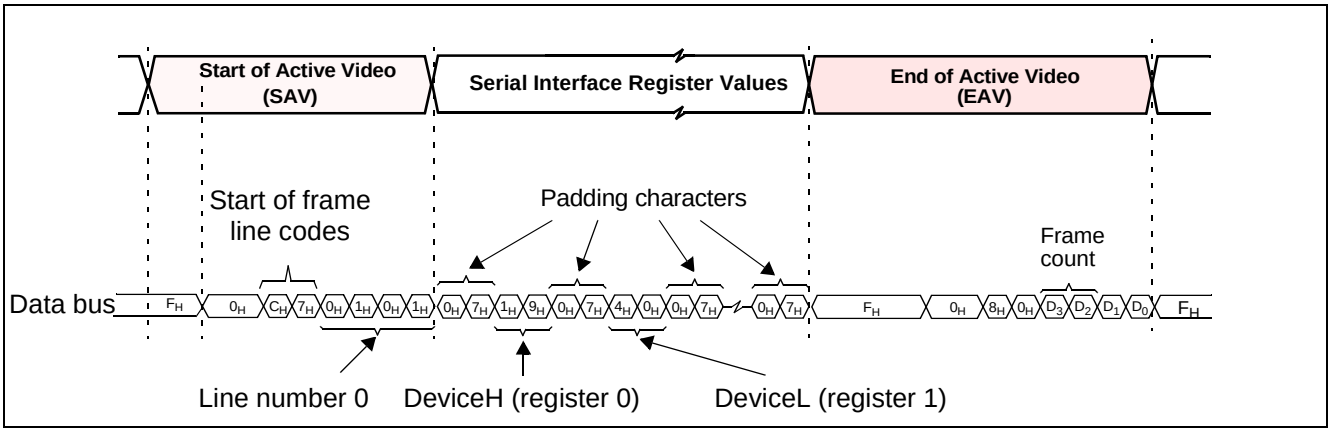
Start of frame line format

The start of frame line contains the contents of the first 16 serial interface registers rather than any video data. This information immediately follows the line code at the beginning of the line. The code 07_H is output after each serial interface value.

It takes 32 pixel clock periods to output these 16 serial interface register values. The remaining pixel periods of the video portion of the line are padded out using 07_H values. The first two pixel locations are also padded with 07_H characters (*Figure 10*). If a serial interface register location is unused then the value from register 0 is output.

Following the escape sequence and line code at the end of active video, a frame count is output.

Figure 10: Start of frame line format



Active video line format

All video data is contained on active video lines. The pixel data appears as a continuous stream of bytes within the active lines.

Black line format

The black lines contain information from the sensor black lines (held in zero exposure). This information may be used by certain co-processors.

Dark line format

The dark lines contain information from the sensor dark lines (shielded from light by metal). The information from these lines is used by the sensor to calculate a dark average offset value which is then applied to the video data to ensure a known ‘black’ level for image data.

Blank line format

To reduce the frame rate it is possible to extend the frame length by adding blank data lines. These contain no video or black line data. In default VGA mode there are no blank lines.

End of frame line format

The end of frame line sole purpose is to indicate the end of a frame, it contains no video data.

Line Duration

Table 4 shows the image duration and interline intervals with default setup.

Table 4: Line timing

Sensor Clock	Pixel Clock	Image		Interline		Line Total	
		QCKs	µs	QCKs	µs	QCKs	µs
24MHz	12MHz	644	53.6	118	9.8	762	63.5

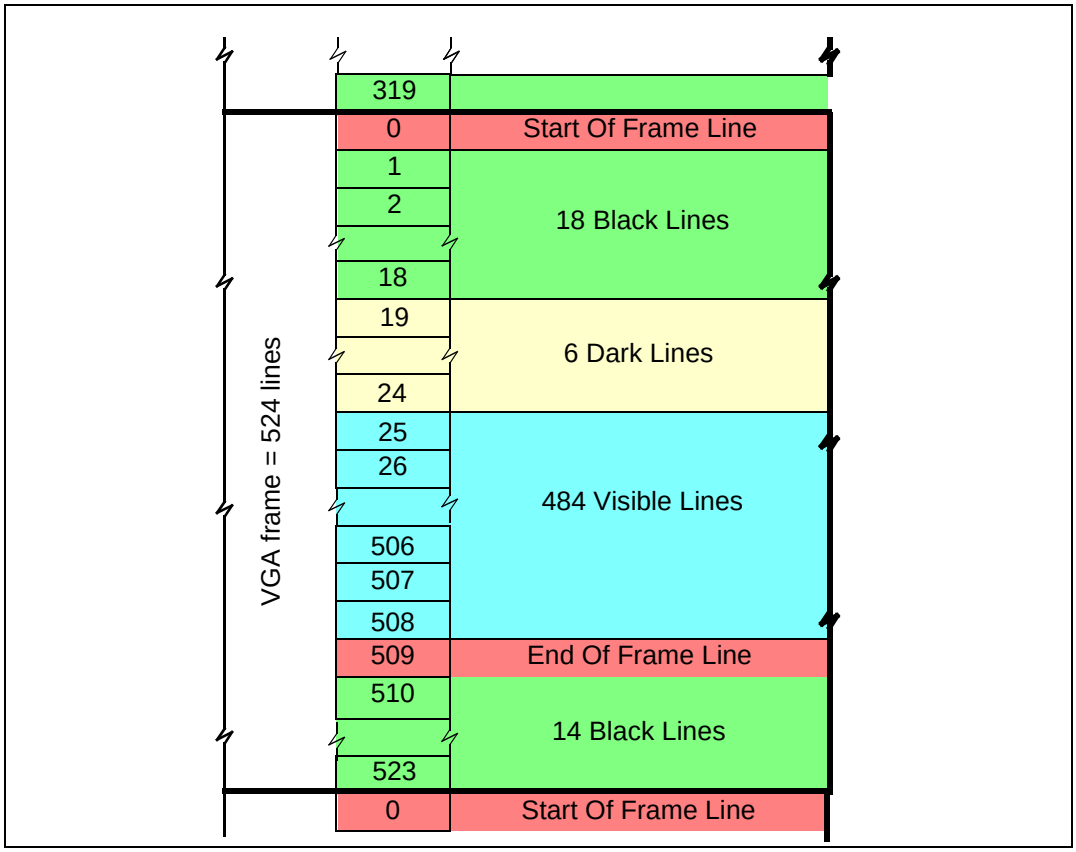
Extending line lengths

The user can extend the line length by writing to serial registers 82 and 83. The line length padding is inserted after the EAV sequence, ensuring that the distance between the SAV and EAV sequences remains constant.

3.1.7 Frame format

Each video frame is composed of a sequence of data lines as illustrated in *Figure 11*.

Figure 11: VGA frame format



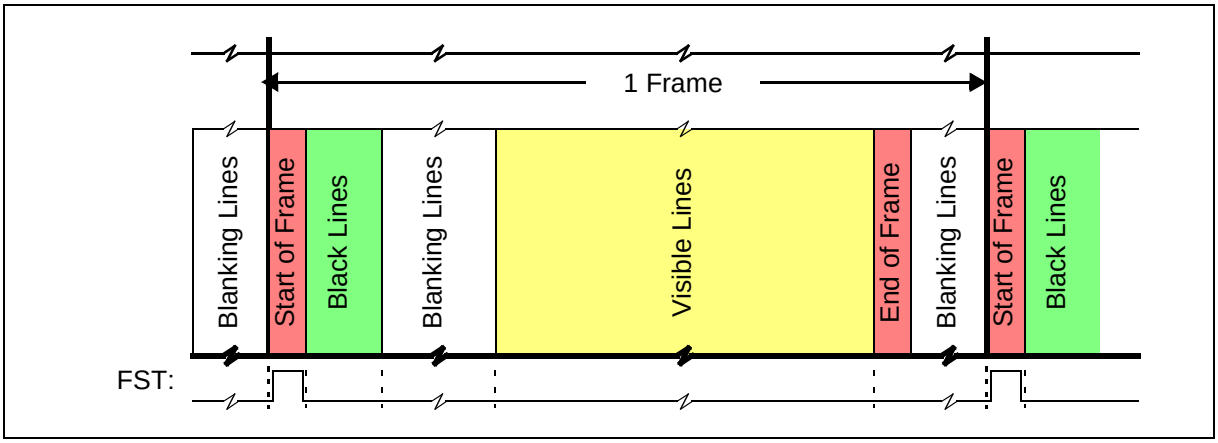
Extending the inter-frame period

The user may choose to extend the inter-frame period by increasing the frame length by writing to serial registers 97 and 98. In this event, the appropriate number of additional blank lines is inserted between the End Of Frame (EOF) line and the Start Of Frame (SOF) line. This means that the distance between SOF and EOF remains constant.

Timing of Frame Start signal (FST)

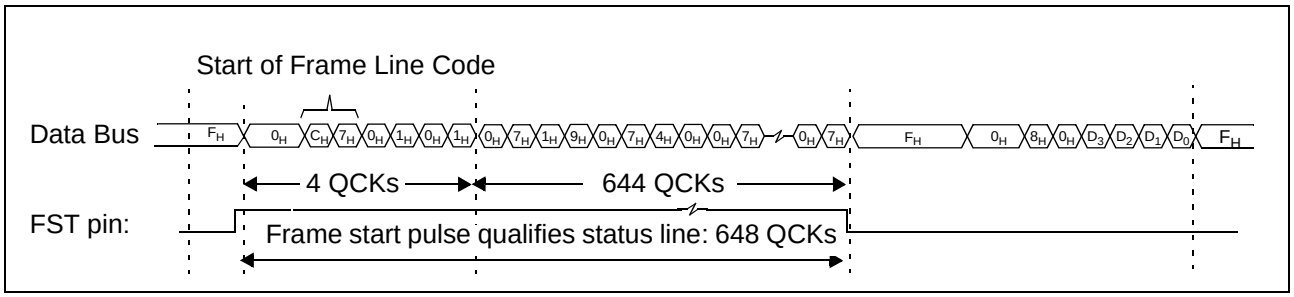
The frame-level position of FST is illustrated in *Figure 12*.

Figure 12: FST timing overview



The FST pulse qualifies the Status Line information and is 648 QCKs (slow) long.

Figure 13: Detailed FST timing

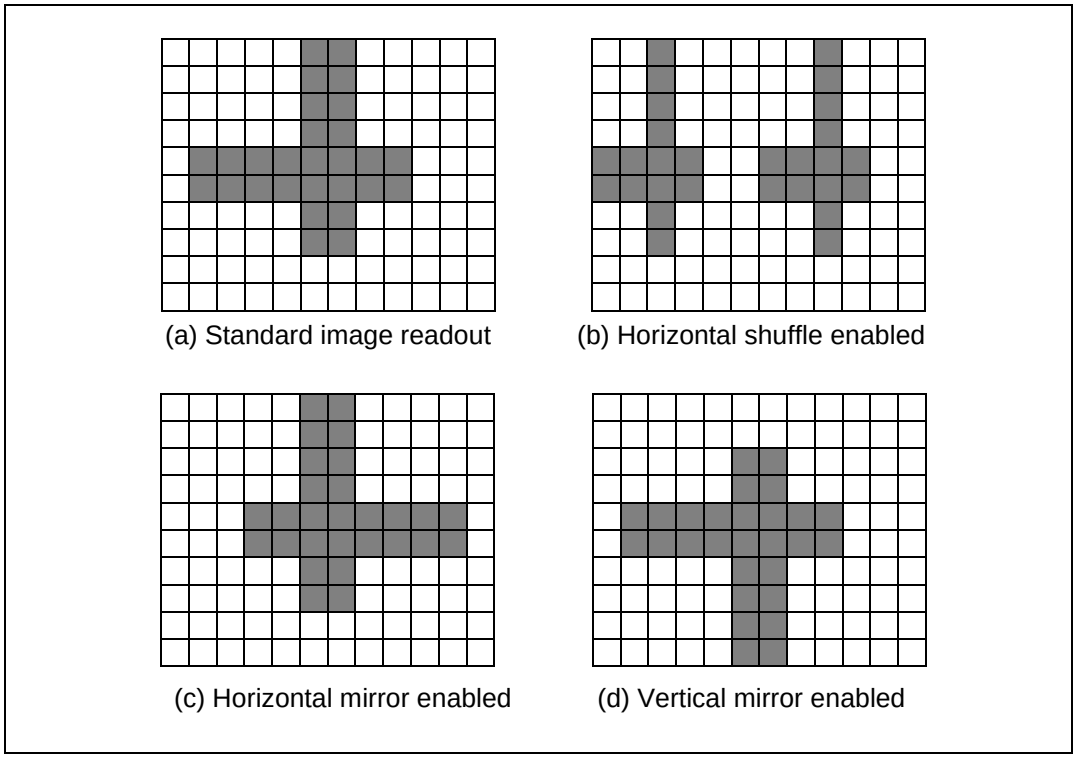


3.1.8 Image translations

The imaging array can be readout with different modes as described here below:

- Shuffle horizontal readout, bit [7] of serial register [17]. Even columns (2,4,6.) are readout first.
- Mirror horizontal readout, bit [3] of serial register [22]. Columns are readout in reverse order.
- Mirror vertical readout, enabled by setting [4] of serial register [22]. Rows are readout in reverse order.

Figure 14: Image readout modes



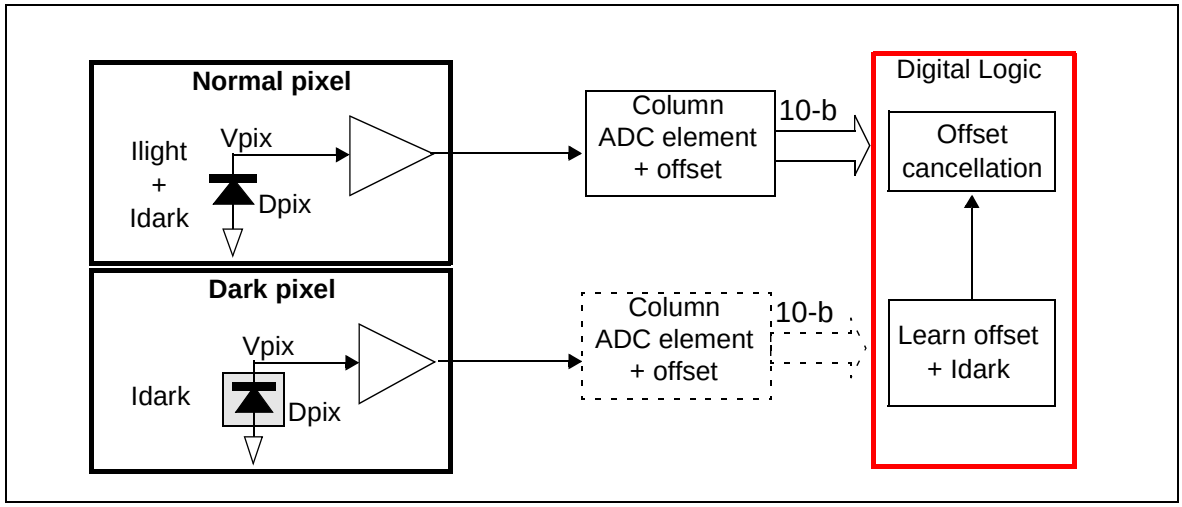
3.1.9 Dark calibration

In order to produce a high quality output image from the VV6501, it is necessary to accurately control the black level of the video signal. There are two main sources of error:

- Dark current
- Offsets in the output path.

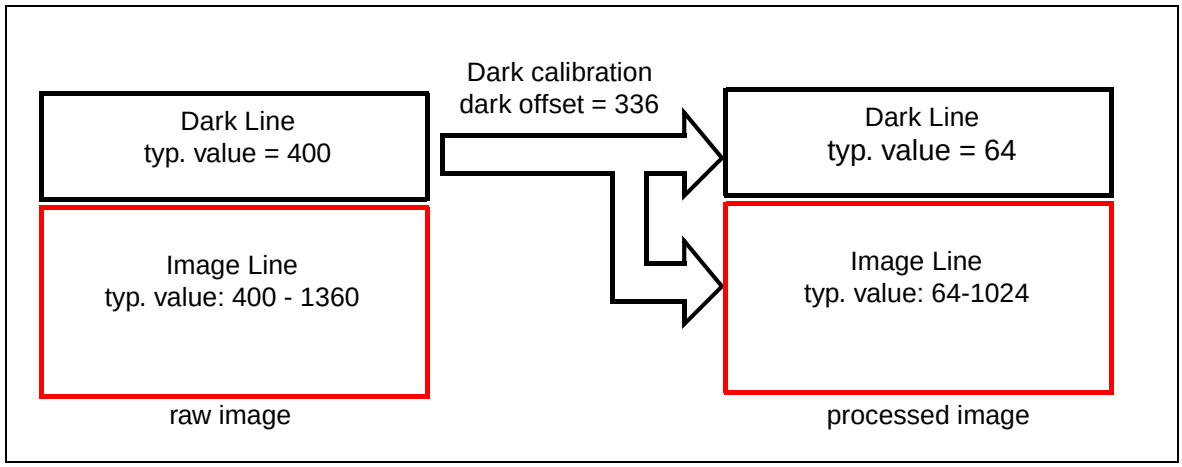
The black level is corrected by using dark pixel rows to “learn” the offset so that it can then be subtracted from the image data. Dark rows have the same exposure setting as the visible lines but are shielded from incident light.

Figure 15: Overview of dark offset cancellation



For 10-b data the ideal “black” code is set to be 64 (when viewing 8-b data the ‘black’ code should be 16). The aim of the dark calibration algorithm is to “learn” the offset required such that “black” image lines have code 64.

Figure 16: Role of dark offset calibration



Dark calibration algorithm

The dark line monitoring logic accumulates a number of dark pixels, calculates an average and then compares this average with the appropriate black level. There is a bit in serial register 45 which determines whether the offset applied is the user-programmable value from serial register 44, or the value calculated by the offset cancellation processor.

The dark offset cancellation algorithm accumulates data from the dark lines which is input to a leaky integrator and an appropriate offset is calculated.

Following an exposure/gain change, on power up or when going out of suspend mode, the history in the dark calibration leaky integrator is reset to the incoming value as the previously stored value will be out of date.

User control

The serial interface allows the user the following additional controls:

- Accumulate dark pixels, calculate dark pixel average and report, but do not apply anything to data stream
- Accumulate dark pixels, calculate dark pixel average, report and apply internally calculated offset to data stream
- Accumulate dark pixels, calculate dark pixel average and report, but apply a SIF supplied offset

3.1.10 Sensor clock and frame rate control

The frame rate is determined by both the input sensor clock and some additional registers under user control.

Sensor clock

The sensor requires a single-ended clock input. A 24MHz clock is required to generate 30 frames per second VGA images. The results is a pixel rate of 12MHz.

Slower frame rates

In order to achieve slower frame-rates the user has a number of options:

- increase the inter-frame time by adding blank line (via SIF register)
- apply a slower external clock
- divide down the external clock using the sensor internal clock divider (via SIF register)

Clock divider

The sensor contains a 4-bit register with which the user selects the clock divider setting (N). *Table 5* gives the mapping between the clk_div value and the divider ratio.

Table 5: User programmable clock divider values

clk_div[3:0]	divide by
0000 [default]	1
0001	2
001X	4
010X	6
011X	8
100X	10

Table 5: User programmable clock divider values

clk_div[3:0]	divide by
101X	12
110X	14
111X	16

3.1.11 Exposure/gain control

The sensor does not contain any form of automatic exposure or gain control. To produce a correctly exposed image, exposure and gain values must be calculated externally and written to the sensor via the serial interface.

Exposure calculation

The exposure time for a pixel and the ADC range (therefore the gain) are programmable via the serial interface. The explanation below assumes that the gain and exposure values are updated together as part of a 5 byte serial interface auto-increment sequence.

Exposure time combines coarse, fine exposure, pixel rate also related to frame and line lengths, all defined in *Table 6*.

Table 6: Definitions related to exposure

Frame length	Number of lines per frame [default=524] The frame length may be increased to 1023 by writing to the frame length register.
Line length	Number of pixels in a line [default = 762] The line length may be increased to 1023 by writing to the line length register.
Exposure	The pixel exposure time is determined by the course and fine exposure values
Coarse exposure value	The number of lines a pixel exposes for. Limited by frame length. Coarse exposure value is in the range [0 - (frame length -2)].
Fine exposure value	Number of additional pixel periods a pixel exposes for. Limited by line length. Fine exposure value is in the range [11 - (line length)].
Pixel period	Determined by the input clock frequency (Fclkin) and user clk_div setting. PixPeriod=(2*N)/Fclkin where N = clock divider ratio
Exposure time	PixPeriod x [($Coarse_{num\_lines}$ x $Line\_Length_{num\_pixels}$) + $Fine_{pixels}$]

Example of exposure calculation in default VGA video mode

coarse exposure = 522

fine exposure = 762

Input clock frequency - Fclkin = 24MHz,

Pixel period = $2/(24 \times 10^6) = 8.33 \times 10^{-8}$ s

Calculation: exposure time = $8.33 \times 10^{-8} \times [(522 \times 762) + 762] = 33.2$ ms

The available range of exposure (without using clock division) is shown in *Table 7*.

Table 7: Exposure ranges [24MHz system clock]

Range	Coarse (no. lines)	Line length (no. pixels)	Fine (no. pixels)	Exposure	
				No. pixels	Time
Min.	0	762	11	0	0.92 µs
Max (default-VGA)	522	762	762	400,050	33.2 ms
Max (available)	1023	1023	1023	$1023^2 + 1023$	87.3 ms

3.1.12 Gain timing and exposure updates

Exposure and gain values are re-timed within the sensor to ensure that a new set of values is only applied to the sensor array at the start of each frame. Bit 0 of the status register is set high when a new exposure value is written via the serial interface but has not yet been applied to the sensor array.

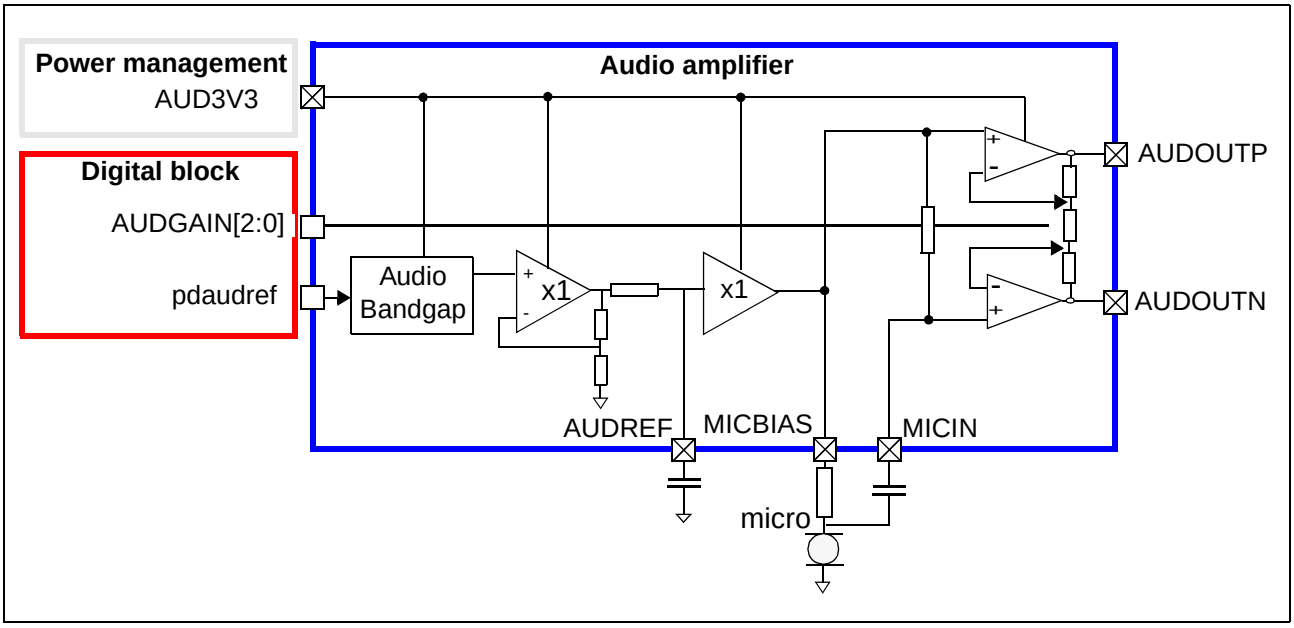
There is a 1 frame latency between a new exposure value being applied to the sensor array and the results of the new exposure value being read-out. The same latency does not exist for the gain value. To ensure that the new exposure and gain values are aligned up correctly the sensor delays the application of the new gain value by one frame relative to the application of the new exposure value.

To eliminate the possibility of the sensor array seeing only part of the new exposure and gain settings, if the serial interface communication extends over a frame boundary, the internal re-timing of exposure and gain data is disabled while writing data to any location in the exposure page of the serial interface register map. Thus, if the 5 bytes of exposure and gain data is sent as an auto-increment sequence, it is not possible for the sensor to consume only part of the new exposure and gain data.

3.2 Audio block

The audio amplifier is designed to drive an external ADC, possibly in the co-processor, with an amplified audio signal taken from a FET microphone input. The 3-bit gain control and power down for the reference are controlled via the I^2C interface.

Figure 17: VV6501 audio amplifier overview



3.2.1 Co-processor support for audio

Table 8 below summarizes the audio capability of the different co-processors the VV6501 is intended to work with.

Table 8: Co-processor support for audio

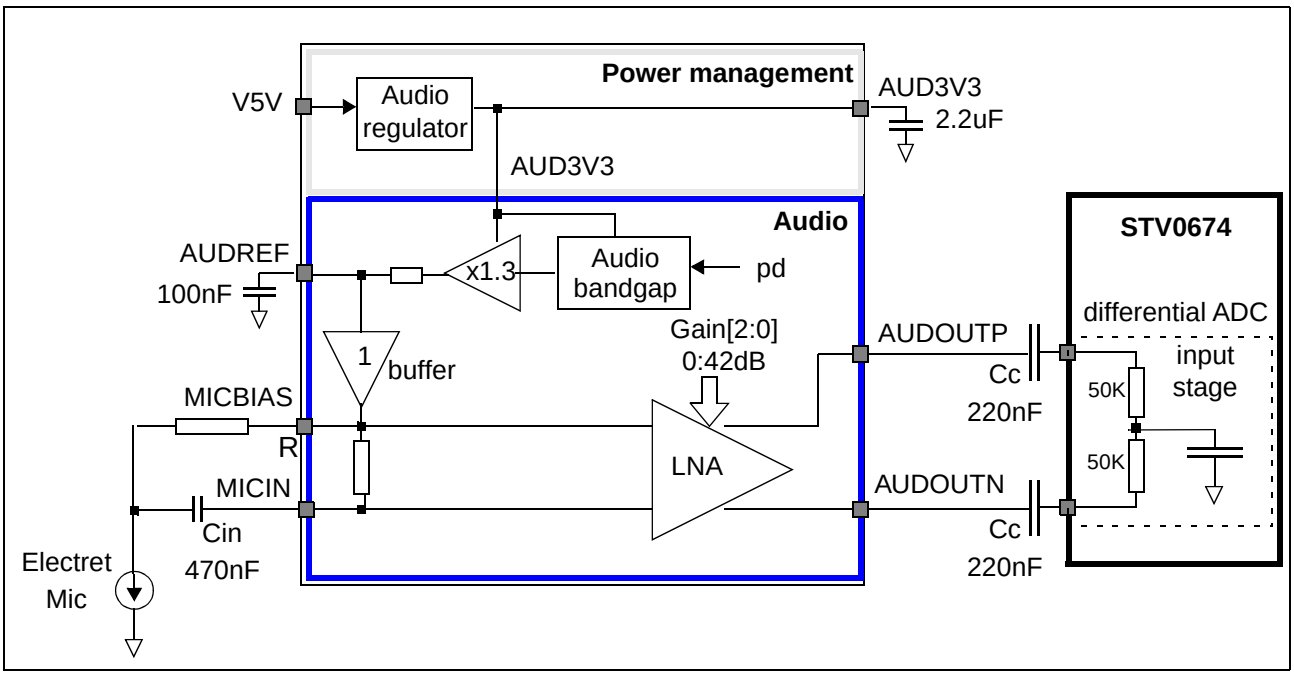
Co-processor	Audio support	Comment
STV0676	Audio 8-b digital endpoint	External ADC needed
STV0674	16 bit Sigma-Delta	501 audio output is directly AC coupled to STV0674 differential audio inputs. STV0674 includes digital ALC and noise gate
STV0680/1	Successive approximation ADC	Low quality audio recording support

3.2.2 Audio amplifier key features

- Very high PSRR micro bias reference due to bandgap from the 3.3V regulated supply, as well as RC network for LF filtering in the audio bandwidth.
- Fully differential low-noise amplifier with gain control via serial IF (0dB to +42dB in 6dB steps).

Up to 1.8Vpp dynamic range on AUDOUTP and AUDOUTN

Figure 18: VV6501 audio amplifier in typical application



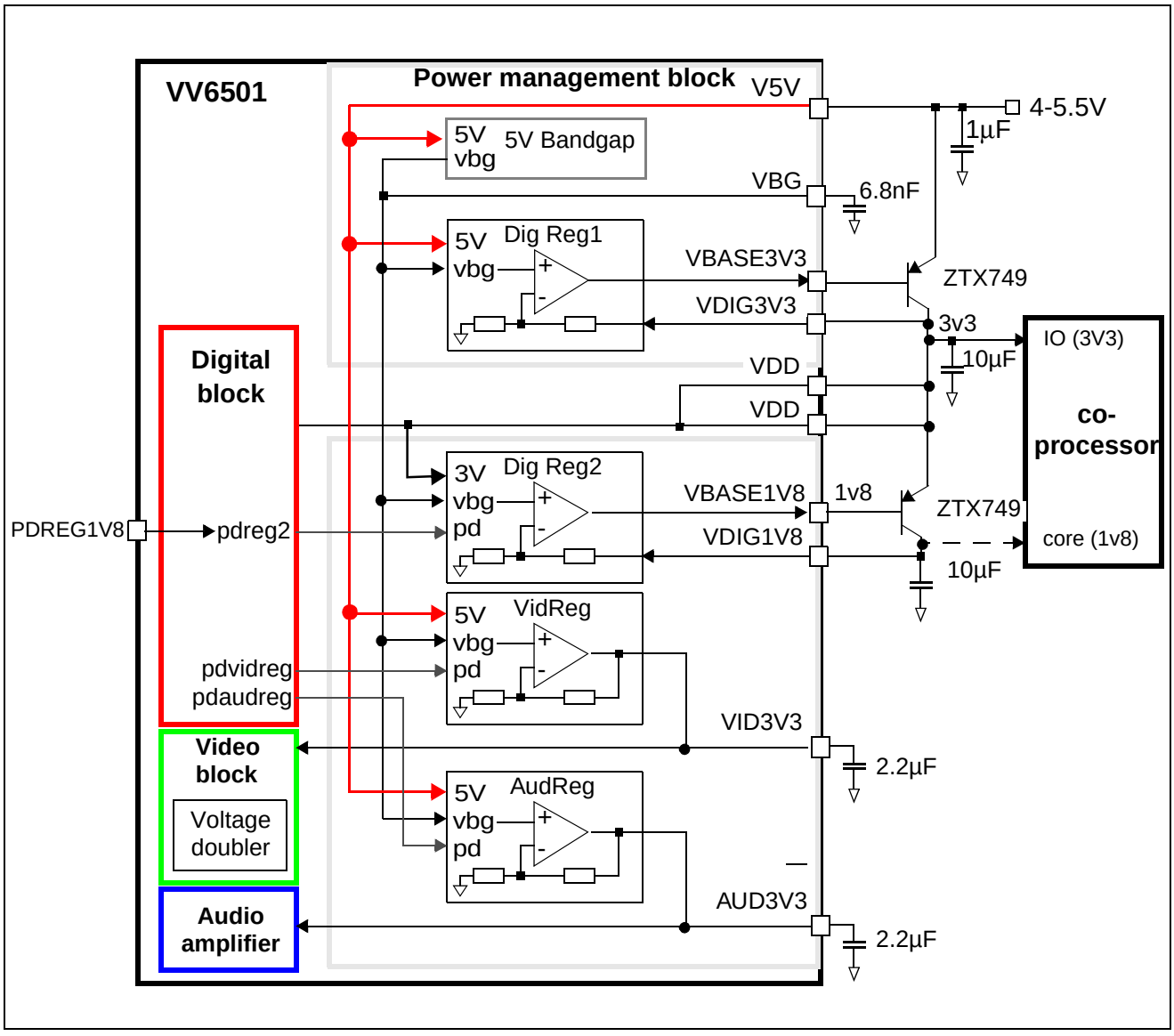
3.3 Power management

3.3.1 Voltage regulators

The power management block on the device avoids the requirement for any external system regulators in a 5 V based camera product. The scheme is shown in *Figure 19*.

- Digital Regulator 1 - This 5 V to 3.3 V regulator uses an external bipolar transistor to supply loads up to 200 mA. It is typically used to power the sensor digital logic and may also be used to supply an external co-processor if required. This regulator is **always** on.
- Digital Regulator2 - This 3.3 V to 1.8 V regulator uses an external bipolar transistor to supply loads up to 100 mA. This supply may be used for an external co-processor if required. This regulator is controlled by the PDREG1V8 pin and must be switched off if not required.
- Audio Amp Regulator - This 5 V to 3.3 V regulator supplies the audio amplifier and the buffer amplifier used to supply the reference to the microphone (Load 5 mA). It should be externally decoupled with a 2.2 µF capacitor. For applications without audio this regulator may be powered down via the SIF registers.
- Video Regulator - This 5 V to 3.3 V regulator supplies the analogue video circuitry. It should be externally decoupled with a 2.2 µF capacitor.

Figure 19: Voltage regulator block diagram

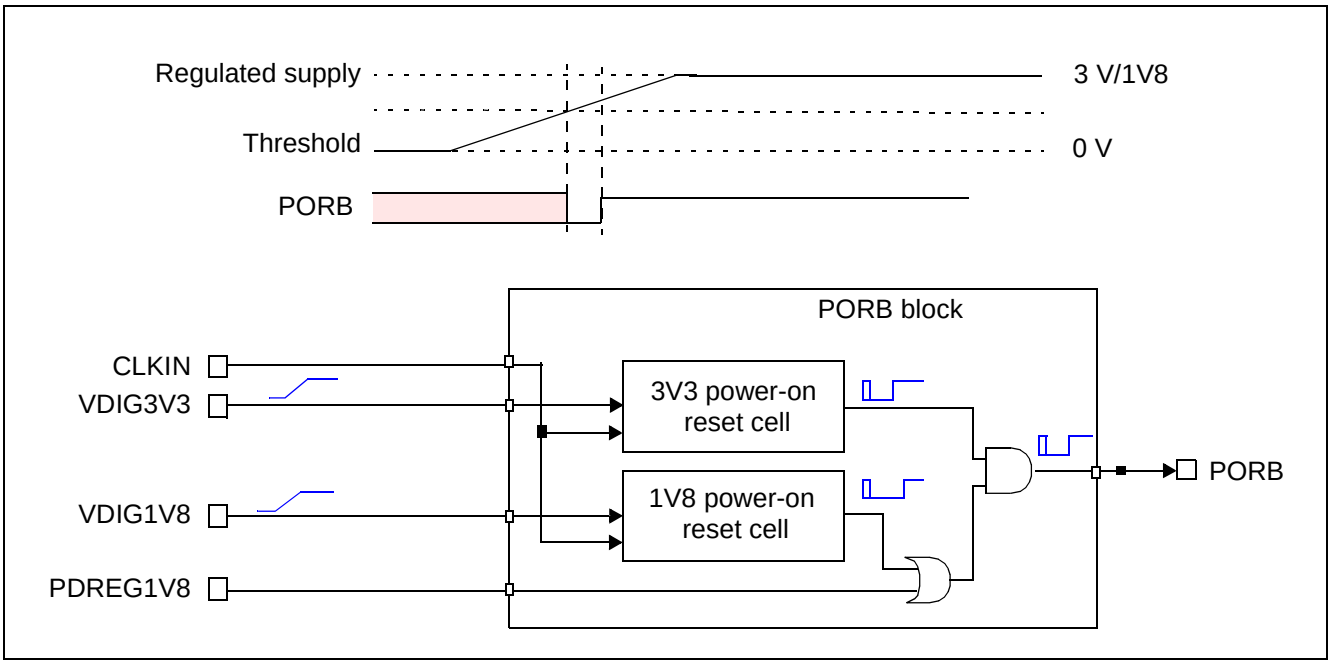


3.3.2 Power-on reset cell

The power-on reset cell generates a low going pulse whenever the digital power supplies are below their lower limits. The power-on reset signal resets the sensor internally and is also available on the PORB pin and may be used to reset a co-processor.

The PORB cell monitors both the 3V3 and 1V8 supplies. If the 1V8 supply is not required then PDVREG1V8 must be tied high.

Figure 20: Power-on reset block



3.4 Device operating modes

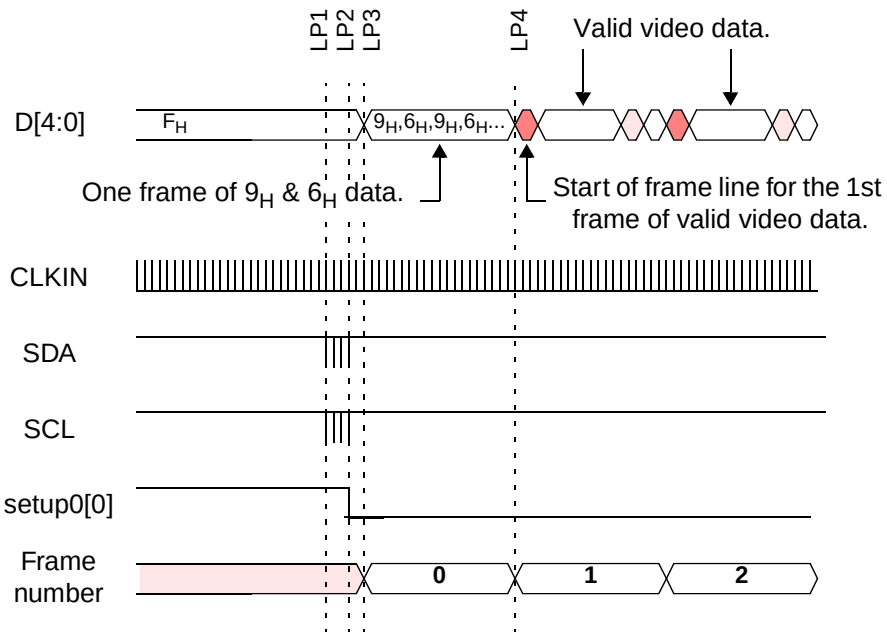
3.4.1 Power-up

On power up the sensor is in low-power mode. All data bus lines drive high to indicate that the device is “present”.

3.4.2 Waking up the sensor

The sensor is made to exit low power mode by enabling the external clock and writing to SIF register16 bit 0. The first frame output after exiting low-power mode does not contain any valid video data.

Figure 21: Exiting low-power mode



LP1	D[4:0] are set to F_H and the sensor analogue circuitry is powered down.
LP2-LP3	“Exit low power mode” command. Powers-up analogue circuits and initiates the 1 frame start-up sequence
LP3-LP4	1 frame of alternating 9_H & 6_H data on D[4:0] The sensor is being initialized during this frame.

3.4.3 Low power mode

Entering low-power mode during video streaming causes the analogue circuits to be powered down. The values of the serial interface registers is preserved.

3.4.4 Suspend mode

Suspend mode is the lowest possible power consumption mode with current < 100 µA. In suspend mode the external clock is gated inside the device and the analogue blocks are powered down.

The sensor is set into suspend mode by driving the SUSPEND pin high.

To achieve the lowest possible power consumption, the clock source should also be turned OFF for the duration of the SUSPEND mode.

3.4.5 Sensor soft reset

All the serial interface registers may be reset to their default values by setting the “soft reset” bit (bit 2) of setup register 0. This causes the sensor to enter low power mode.

4 Serial Control Bus

4.1 General description

The 2-wire I2C serial interface bus is used to read and write the sensor control registers.

Some status registers are read-only.

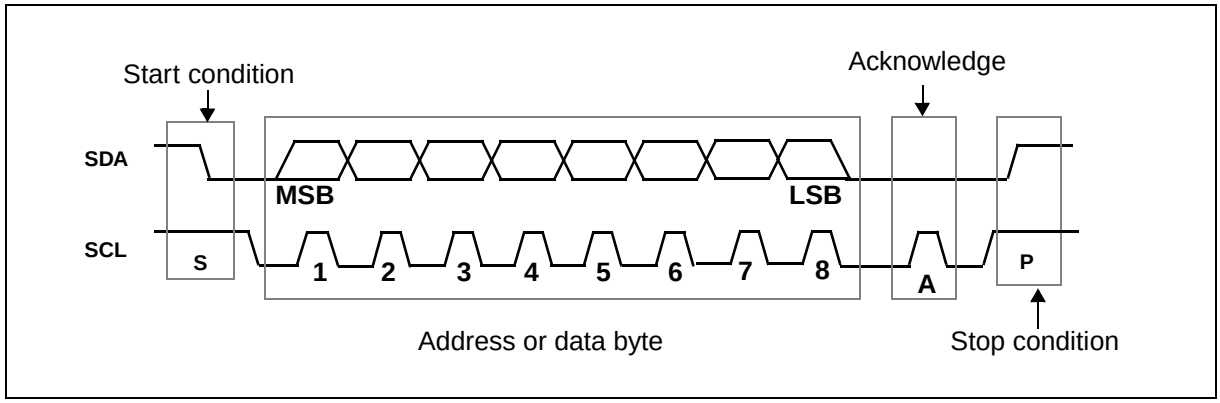
The main features of the serial interface include:

- Variable length read/write messages.
- Indexed addressing of information source or destination within the sensor.
- Automatic update of the index after a read or write message.
- Message abort with negative acknowledge from the master.
- Byte oriented messages.

4.2 Serial communication protocol

The co-processor must perform the role of communication ‘master’ and the sensor acts as a ‘slave’. The communication from host to sensor takes the form of 8-bit data with a maximum serial clock frequency of 100 kHz. Since the serial clock is generated by the bus master it determines the data transfer rate. Data transfer protocol on the bus is illustrated in *Figure 22*.

Figure 22: Serial Interface data transfer protocol



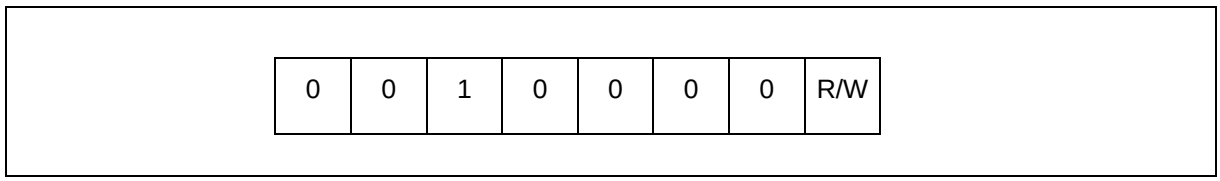
4.2.1 Data format

Information is packed in 8-bit packets (bytes) always followed by an acknowledge bit. The internal data is produced by sampling *sda* at a rising edge of *scl*. The external data must be stable during the high period of *scl*. Exceptions to this are *start* (S) or *stop* (P) conditions when *sda* falls or rises respectively, while *scl* is high.

A message contains at least two bytes preceded by a *start* condition and followed by either a *stop* or *repeated start, (Sr)* followed by another message.

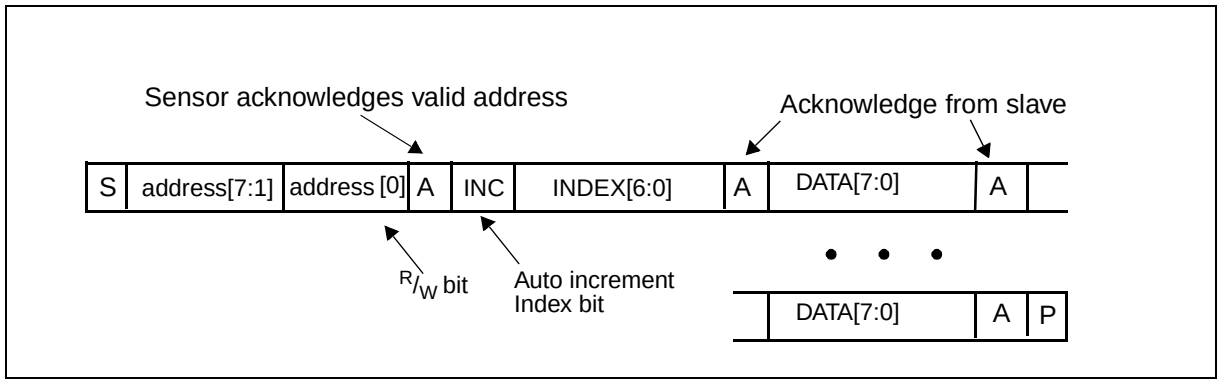
The first byte contains the device address byte which includes the data direction *read,* (r)*, ~write*, (~w), bit.

Figure 23: VV6501 Serial interface address



The byte following the address byte contains the address of the first data byte (also referred to as the *index*). The serial interface can address up to 128 byte registers. If the MSB of the second byte is set, the automatic increment feature of the address index is selected.

Figure 24: Serial interface data format



4.2.2 Message interpretation

All serial interface communications with the sensor must begin with a *start* condition. If the *start* condition is followed by a valid address byte then further communications can take place. The sensor will acknowledge the receipt of a valid address by driving the *sda* wire low. The state of the *read/~write* bit (LSB of the address byte) is stored and the next byte of data, sampled from *sda,* can be interpreted.

During a write sequence the second byte received is an address index and is used to point to one of the internal registers. The MSB of the following byte is the *index auto increment* flag. If this flag is set then the serial interface will automatically increment the index address by one location after each slave acknowledge. The master can therefore send data bytes continuously to the slave until the slave fails to provide an acknowledge or the master terminates the write communication with a *stop* condition or sends a *repeated start*, *(Sr)*. If the auto increment feature is used the master does *not* have to send indexes to accompany the data bytes.

As data is received by the slave, it is written bit by bit to a serial/parallel register. After each data byte has been received by the slave, an acknowledge is generated, the data is then stored in the internal register addressed by the current index.

During a read message, the current index is read out in the byte following the device address byte. The next byte read from the slave device are the contents of the register addressed by the current index. The contents of this register are then parallel loaded into the serial/parallel register and clocked out of the device by *scl.*

At the end of each byte, in both read and write message sequences, an acknowledge is issued by the receiving device. Although VV6501 is always considered to be a slave device, it acts as a transmitter when the bus master requests a read from the sensor.

At the end of a sequence of incremental reads or writes, the terminal index value in the register will be one *greater* than the last location read from or written to. A subsequent read will use this index to begin retrieving data from the internal registers.

A message can only be terminated by the bus master, either by issuing a stop condition, a repeated start condition or by a negative acknowledge after reading a complete byte during a read operation.

4.3 Types of messages

This section gives guidelines on the basic operations to read data from and write data to the serial interface.

The serial interface supports variable length messages. A message may contain no data bytes, one data byte or many data bytes. This data can be written to or read from common or different locations within the sensor. The range of instructions available are detailed below.

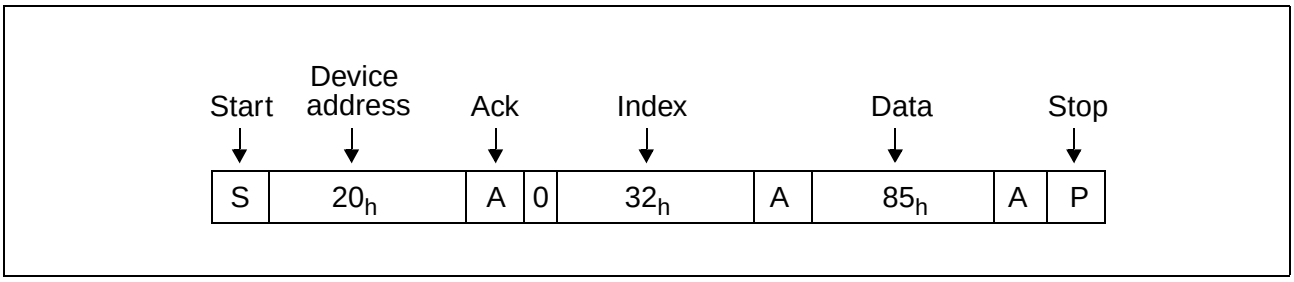
- Write no data byte, only sets the index for a subsequent read message.
- Multiple location write (using auto increment index bit) for fast information transfers.

Examples of these operations are given below. A full description of the internal registers is given in the previous section. For all examples, the slave address used is 32_{10} for writing and 33_{10} for reading. The write address includes the read/write bit (the LSB) set to zero while this bit is set in the read address.

4.3.1 Single location, single data write

When a random value is written to the sensor, the message looks as shown in *Figure 25*.

Figure 25: Single location, single write

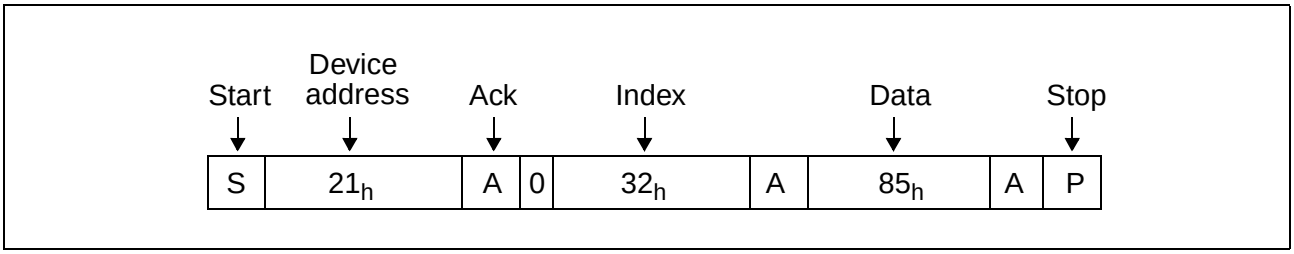


In this example, the *fineH* exposure register (index = 32_{10}) is set to 85_{10}. The r/w bit is set to zero for writing and the *Inc.* bit (MSB of the index byte) is set to zero to disable automatic increment of the index after writing the value. The address index is preserved and may be used by a subsequent read. The write message is terminated with a stop condition from the master.

4.3.2 Single location, single data read

A read message always contains the index used to get the first byte.

Figure 26: Single location, single read

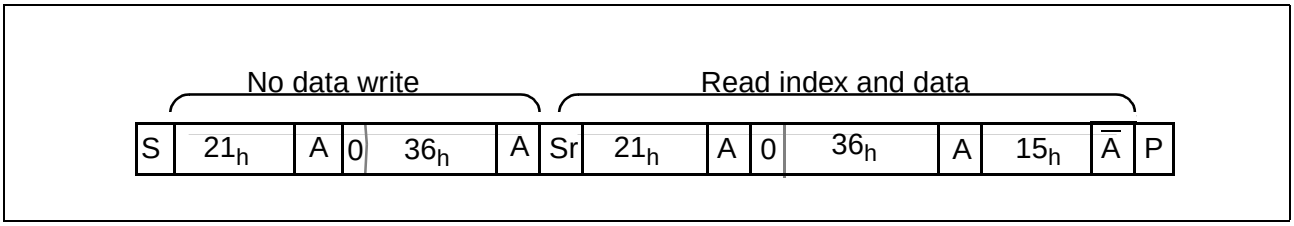


This example assumes that a write message has already taken place and the residual index value is 32_{10}. A value of 85_{10} is read from the *fineH* exposure register. Note that the read message is terminated with a negative acknowledge ($\overline{A}$) from the master: it is not guaranteed that the master will be able to issue a stop condition at any other time during a read message. This is because if the data sent by the slave is all zeros, the *sda* line cannot rise, which is part of the stop condition.

4.3.3 No data write followed by same location read

When a location is to be read and the value of the stored index is not known, a write message with no data byte must be written first, specifying the index. The read message then completes the message sequence. To avoid relinquishing the serial to bus to another master, a repeated start condition is asserted between the write and read messages. In this example, the *gain* value (index = 36_{10}) is read as 15_{10} (see *Figure 27*).

Figure 27: No data write followed by same location read

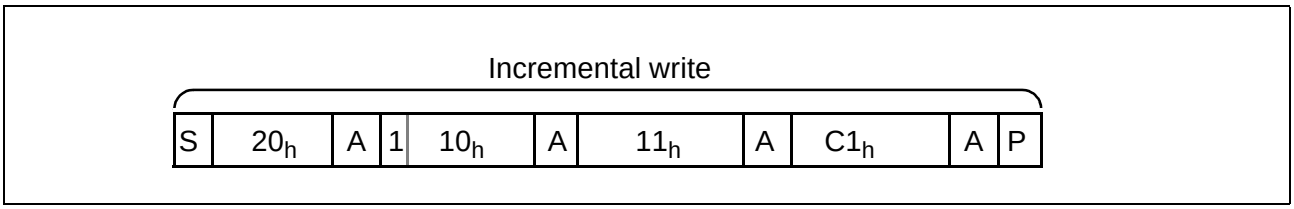


As mentioned in the previous example, the read message is terminated with a negative acknowledge ($\overline{A}$) from the master.

4.3.4 Multiple location write

If the automatic increment bit is set (MSB of the index byte), it is possible to write data bytes to consecutive adjacent internal registers without having to send explicit indexes prior to sending each data byte. An auto-increment write to the exposure registers with their default values is shown in *Figure 28*.

Figure 28: Multiple location write



5 I2C Registers

5.1 Register map

Sensor registers may be split into 5 main categories:

- Status Registers (read only)
- Setup registers with bit significant functions
- Exposure parameters that influence output image brightness
- Video timing functions
- Audio functions

Any internal register that can be written to can also be read from. There are a number of read only registers that contain device status information, (for example design revision details).

Names that end with H or L denote the most or least significant part of the internal register. Note that unused locations in the H byte are packed with zeroes.

A detailed description of each register follows. The address indexes are shown as decimal numbers in brackets [ ]. Note that there are many unused register locations.

Table 9: Serial interface address map

Index	Name	Length	R/W	Default	Comments
Status registers					
0x00	deviceH	8	RO	0x1F	Chip identification number including revision indicator (501 Rev0).
0x01	deviceL	8	RO	0x50	
0x02	status0	8	RO	0x10	Status information
0x09	dark_avgH	4	RO	0	This is the average pixel value returned from the dark line offset cancellation algorithm (2's complement notation)
0x0A	dark_avgL	8	RO	0	
0x0E	frame counter	8	RO		Current frame count (0-255)
Setup registers					
0x10	setup0	8	R/W	0x1	Low-power and video timing
0x11	setup1	8	R/W	0x80	Various parameters
0x14	fg_modes	8	R/W	0	FST and QCK setup
0x15	pin_mapping	7	R/W	0	FST and QCK mapping modes
0x16	vshuffle/mirrors	8	R/W	0	Read-out order of data
0x17	op_format	7	R/W	0x18	Output coding formats
Exposure registers					
0x20	fineH	2	R/W	0	Fine exposure
0x21	fineL	8	R/W		
0x22	coarseH	2	R/W	0x20A	Coarse exposure
0x23	coarseL	8	R/W		
0x24	analogue gain	4	R/W	0	Analogue gain setting
0x25	clk_div	4	R/W		Clock division
0x2C	dark offsetH	3	R/W	0	Dark line offset cancellation value (2's complement notation)
0x2D	dark offsetL	8	R/W		
0x2E	dark offset setup	3	R/W	0x61	Dark line offset cancellation enable
Video timing registers					
0x52	line_lengthH	2	R/W	0x2F9	Line length (pixel clocks)
0x53	line_lengthL	8	R/W		
0x54	frame_lengthH	2	R/W	0x20B	Frame length (lines)
0x55	frame_lengthL	8	R/W		
Audio register					
0x79	audio	4	R/W	0x9	Audio setup register

5.2 Register description

5.2.1 Status registers

[0x00-0x01] - DeviceH and DeviceL

These registers provide read only information to identify the sensor type that has been coded as a 12-bit number and a 4-bit mask set revision identifier. The device identification number for VV6501 is 501 equivalent to 0001 1111 0101_2. The initial mask revision identifier is 0 equivalent to 0000_2.

Table 10: [0x00] - DeviceH

Bits	Function	Default	Comment
[7:0]	Device type identifier	0x1F	Most significant 8 bits of the 12 bit code identifying the chip type.

Table 11: [0x01] - DeviceL

Bits	Function	Default	Comment
[7:4]	Device type identifier	0x5	Least significant 4 bits of the 12 bit code identifying the chip type.
[3:0]	Mask set revision identifier	0	

[0x02] - Status0

Bit	Function	Default	Comment
7	Video timing parameter update pending flag	0	Video timing parameters sent but not yet consumed by sensor
[6:5]	RESERVED		
4	Odd/even frame	0x1	The flag will toggle state on alternate frames
3	Clock division update pending	0	Clock divisor sent but not yet consumed by the sensor
2	Gain value update pending	0	Gain value sent but not yet consumed by the sensor
1	Coarse exposure value update pending	0	Coarse exposure value sent but not yet consumed by the sensor
0	Fine exposure value update pending	0	Fine exposure value sent but not yet consumed by the sensor

[0x09-0x0A] - Dark_Avg

Register Index	Bits	Function	Default	Comment
10	[7:0]	Dark avg ls byte	0	The calculated pixel average over a series of dark lines.
9	[1:0]	Dark avg ms bits	0	

[0x0E] - Frame Counter

Register index	Bits	Function	Default	Comment
14	[7:0]	Frame count	0	Increments by 1 at each frame

5.2.2 Setup Registers

[0x10] - Setup0

Bit	Function	Default	Comment
[7:5]	Video Timing Mode	0x1	VGA Mode
[4:3]	RESERVED		
2	Soft Reset **Off** / On	0	Setting this bit resets the sensor to its power-up defaults. This bit is also reset.
1	RESERVED		
0	Low Power Mode: Off / **On**	0x1	Powers down the sensor array and audio. The output data bus goes to F_H. On power-up the sensor enters low power mode.

[0x11] - Setup1

Bit	Function	Default	Comment
7	Pixel read-out order (hshuffle) Unshuffled or **Shuffled**	1	Shuffle is enabled by default
[6:5]	RESERVED		
4	Enable immediate gain update. **Off**/On	0	Allow manual change to gain to be applied immediately
3	Enable immediate clock division update. **Off**/On	0	Allow manual change to clock division to be applied immediately
[2:0]	RESERVED		

[0x14] - fg_modes

Bit	Function	Default	Comment
[7:6]	FST mode	0	0 - Off 1 - On - qualifies the status line
[5:4]	RESERVED		
[3:2]	QCK modes	0	00 - Off 01 - Free running 1x - Valid during data period only
1	RESERVED		
0	QCLK type	0	0 - **slow_QCLK/** 1 - fast_QCLK

[0x15] - pin_mapping

Bit	Function	Default	Comment
7	RESERVED		
6	reset_flag.	1	Set to 1 by porb, reset_n soft_reset. The user can clear this bit by writing to SIF.
5	RESERVED		
[4:3]	RESERVED		
2	Forced value for FST pin	0	only when enabled by bit0
1	Forced value for QCLK pin	0	only when enabled by bit0
0	Map serial interface register bits values on to the QCK and FST pins.	0	Select data to appear on FST and QCK pins 0 - FST and QCK signals (default) 1 - pin_mapping[2] and pin_mapping[1]

[0x16] - Vshuffle/mirrors

Bit	Function	Default	Comment
[7:5]	RESERVED		
4	Line read-out order (vmirror) **Normal** or Mirrored	0	
3	Pixel read-out order (hmirror) **Normal** or Mirrored	0	
[2:0]	RESERVED		

[0x17] - op_format

Bit	Function	Default	Comment
7	RESERVED		
6	Re-time tri-state update. **Off** / On	0	Re-time new tri-state value to a frame boundary.
5	Tri-state output data bus, FST & QCLK **Outputs Enabled** / Tri-state	0	On power up the data bus, QCLK & FST pads are enabled by default.
[4:3]	RESERVED		
2	Embedded SAV/EAV Escape Sequences **On /** Off	0	0 - Insert Embedded Control Sequences e.g Start and End of Active Video into Output Video data 1 - Pass-through mode. Output Video data equals ADC data. Note: also disables FST when SAV/EAV generation disabled.
1	RESERVED		
0	Data format select.	0	0 - 5 wire parallel output 1 - 4 wire parallel output

5.2.3 Exposure control registers

There is a set of programmable registers which control the sensor sensitivity. The registers are as follows:

- Fine exposure
- Coarse exposure time
- Analogue gain
- Clock division

The gain parameter does not affect the integration period rather it amplifies the video signal at the output stage of the sensor core.

Note: The external exposure (coarse, fine, clock division or gain) values do not take effect immediately. Data from the serial interface is read by the exposure algorithm at the start of a video frame. If the user reads an exposure value via the serial interface, then the value reported will be the data as yet unconsumed by the exposure algorithm, because the serial interface logic locally stores all the data written to the sensor.

Between the writing the of exposure data and the use of the data by the exposure logic, bit 0 of the status register is set. The gain value is updated a frame later than the coarse, fine and clock division parameters, since the gain is applied directly at the video output stage and does not require the long set up time of the coarse, fine exposure and of the clock division.

To eliminate the possibility of the sensor array seeing only part of the new exposure and gain settings, if the serial interface communication extends over a frame boundary, the internal re-timing of exposure and gain data is disabled while writing data to any location in the exposure page of the serial interface register map. Thus if the 5 bytes of exposure and gain data is sent as an auto-increment sequence, it is not possible for the sensor to consume only part of the new exposure and gain data.

The range of some parameter values is limited and any value programmed out of the range is clipped to the maximum allowed.

Table 12: Exposure, clock rate and gain registers

Register index	Bits	Function	Default	Comment
0x20	0	Fine MSB exposure value	0	Line length dependent
0x21	[7:0]	Fine LSB exposure value		
0x22	0	Coarse MSB exposure value	0x20A	Frame length dependent. Maximum for default modes: VGA = 522
0x23	[7:0]	Coarse LSB exposure value		
0x24	[7:0]	Analogue gain value	0	Bits[3:0] IDAC control
0x25	[3:0]	Clock divisor value	0	See *[0x25] - Clock divider setting* for details
0x2C	[1:0]	Dark offsetH	0	Dark offset manual settings
0x2D	[7:0]	Dark offsetL	0	
0x2E	[7:0]	Dark offset control register	0	

[0x20] - Fine exposure MSB

Bit	Function	Default	Comment
[7:2]	RESERVED		
[1:0]	Fine Exposure [9:8]	0	

[0x21] - Fine exposure LSB

Bit	Function	Default	Comment
[7:0]	Fine Exposure [7:0]	0	

[0x22] - Coarse exposure MSB

Bit	Function	Default	Comment
[7:2]	RESERVED		
[1:0]	Coarse Exposure [9:8]	0x2	

[0x23] - Coarse exposure LSB

Bit	Function	Default	Comment
[7:0]	Coarse Exposure [7:0]	0xA	Default = 522

[0x24] - Analogue gain/ offset

Bit	Function	Default	Comment
[7:4]	RESERVED		
[3:0]	GAIN [3:0]	0	0000 = 1.0, Min. Gain = (0dB) 0001 = 1.06 0010 = 1.14 0011 = 1.23 0100 = 1.33 0101 = 1.45 0110 = 1.60 0111 = 1.78 1000 = 2.0 1001 = 2.29 1010 = 2.67 1011 = 3.2 1100 = 4.0 1101 = 5.33 1110 = 8.0 1111 = 16, Max Gain = (24dB)

[0x25] - Clock divider setting

Bit	Function	Default	Comment
[7:4]	RESERVED		
[3:0]	Clock divider setting	0	0000 - Divide clock by 1 0001 - Divide clock by 2 001x - Divide clock by 4 010x - Divide clock by 6 011x - Divide clock by 8 100x - Divide clock by 10 101x - Divide clock by 12 110x - Divide clock by 14 111x - Divide clock by 16

[0x2C -0x2D] - Dark line pixel offset

Bit	Function	Default	Comment
[7:0]	LS Dark line pixel offset	0	This register contains a fixed offset that can be applied to the digitised pixels in the digital output coding block. The offset is a 2's complement number, giving an offset range -1024,+1023.
[2:0]	MS Dark line pixel offset		

[0x2E] - Dark line offset cancellation setup register

Bit	Function	Default	Comment
7	RESERVED		
[6:4]	RESERVED		
3	Dark leaky integrator time constant	0	0 - Fast 1 - Slow
2	RESERVED		
[1:0]	Dark line offset cancellation	01	00 - Accumulate dark pixels, calculate dark pixel average and report, but don't apply anything to data stream **01** - Accumulate dark pixels, calculate dark pixel average, report and apply internally calculated offset to data stream 11 - Accumulate dark pixels, calculate dark pixel average and report, but apply an externally calculated offset

5.2.4 Video timing registers

Indexes in the range [0x52 - 0x62] control the line and frame length of the sensor. The registers are as follows:

- line length
- frame length

The line length is specified in a number of pixel clocks, whereas the frame length is specified in a number of lines.The range of some parameter values is limited and any value programmed out of the range is clipped as follows:

- Values greater than the maximum are clipped to the maximum allowed.
- Values less than the default for a given mode are clipped to the default value.

Table 13: Video timing registers

Register index	Bit	Function	Default	Comment
0x53	[7:0]	Line Length LSB value	0xF9	
0x52	[7:2]	RESERVED		
	[1:0]	Line Length MSB value	0x2	Default = 761 Maximum = 1023 (register value is line length - 1)
0x62	[7:0]	Frame Length LSB value	0x0B	
0x61	[7:2]	RESERVED		
	[1:0]	Frame Length MSB value	0x2	Default = 523 Maximum = 1023 (register value is frame length - 1)

5.2.5 Audio setup register

[0x79] - Audio amplifier setup (AT1)

Bit	Function	Default	Comments
7	Retro gain mode select	0	0 - Retro gain mode 1 - Standard gain mode
6	Power down audio ref. only	0	
[5:4]	RESERVED		
3	Power down amp. and ref.	0	0 - Powered up 1 - Power down
[2:0]	Audio amplifier gain	1	

Table 14: Audio gain options

reg121[2:0]	Retro gain mode ([[7]=0)		Standard gain mode ([7]=1)	
	Gain	AUDGAIN[2:0]	Gain	AUDGAIN[2:0]
000	0dB	000	0dB	000
001	30dB	101	6dB	001
010	6dB	001	12dB	010
011	36dB	110	18dB	011
100	12dB	010	24dB	100
101	42dB	111	30dB	101
110	18dB	011	36dB	110
111	24dB	100	42dB	111

6 Electrical Characteristics

6.1 Absolute maximum ratings

Table 15: Absolute maximum ratings

Symbol	Parameter	Max.	Unit
V_{DD}	Regulator input power voltage	-0.5 to 6.0	V
V_{DD}	Digital power supply	-0.5 to 3.6	V
V_{CC}	Analogue power supply	-0.5 to 3.6	V
T_{STO}	Storage temperature[a]	-25 to + 85	^{o}C
T_{LEAD}	Lead temperature (10 s) JDEC moisture level 3	225	°C

a. A temperature below 0°C can induce a slight humidity penetration into the package cavity. This humidity is easily removable by a short storage in standard climatic conditions (25°C/50% relative humidity).

Caution: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6.2 Operating conditions

Table 16: Operating conditions

Symbol	Parameter	Max.	Unit
V_{DD}	Supply voltage	4.1 to 5.5	V
T_A	Ambient temperature	0 to +40	°C

6.3 Thermal data

Table 17: Thermal data

Symbol	Parameter	Value	Unit
Rth(j-a)	Junction/ambient thermal resistance	45	°C/W

6.4 DC electrical characteristics

Over operating conditions unless otherwise specified.

6.4.1 Power supply

Table 18: Power supply characteristics

Symbol	Parameter description	Min.	Typ.	Max.	Unit
V_{BUS}	Power supply range of operation	4	5	5.5	V
I_{VBUS}	Normal mode sensor current consumption (VGA 30 fps - no load on digital regulators)		25	50	mA
I_{SUSP}	Current consumption in SUSPEND mode (SUSPEND pin high) and VDIG1V8 disabled.		65	140	µA

6.4.2 Digital block

Table 19: Digital block electrical characteristics

Symbol	Parameter description	Min.	Typ.	Max.	Unit
CMOS digital inputs					
V_{IL}	Low level input voltage			0.8	V
V_{IH}	High level input voltage	2			V
I_{IL}	Low level input current			-1	µA
I_{IH}	High level input current			1	µA
CMOS digital outputs					
V_{OL}	Low level output voltage			0.2	V
V_{OH}	High level output voltage	2.8			V
Serial interface					
F_{SIF}	Operating frequency range	0		100	kHz

6.4.3 Regulators

Table 20: Electrical characteristics of regulators

Symbol	Parameter description	Min.	Typ.	Max.	Unit
5V bandgap					
V_{BG}	Bandgap voltage	1.08	1.2	1.38	V
I_{BG}	Bandgap current drive capability		10		µA
Digital regulator 1					
V_{DIG3V3}	Regulated output voltage, (I_{LOAD} < 300 mA)	3.0	3.3	3.6	V
I_{LOAD}	Output current drive capability		200	300	mA
PSRR	10 Hz < Freq <10 kHz, C = 1 µF, relative to Vbus voltage swing over operating range	40			dB
Digital regulator 2					
V_{DIG1V8}	Regulated output voltage (I_{LOAD} < 50 mA)	1.62	1.8	1.98	V
I_{LOAD}	Output current drive capability	-	100	200	mA
PSRR	10 Hz < frequency <10 kHz, C = 1 µF, relative to Vbus voltage swing over operating range	40			dB
Audio and video regulators					
V_{VIDEO}	3.3 V video regulator	3.0	3.3	3.4	V
I_{VIDEO}	Video current drive capability		10		mA
V_{AUDIO}	3.3 V audio regulator	3.0	3.3	3.4	V
I_{AUDIO}	Audio current drive capability		5		mA

6.4.4 Audio amplifier

Table 21: Audio amplifier electrical characteristics

Symbol	Parameter description	Min.	Typ.	Max.	Unit
Audio reference					
R_{AUDREF}	Output impedance of audio reference I_{LOAD} < 100 µA		100		kΩ
I_{AUDREF}	Audio reference drive capability		1		µA
Microphone bias					
$V_{MICBIAS}$	Microphone bias voltage	1.4	1.6	1.8	V
$I_{MICBIAS}$	Microphone bias drive capability		500		µA
$R_{MICBIAS}$	Micro biasing voltage output impedance ($I_{MICBIAS}$ < 500 µA)		100		W
Microphone input					
R_{MICIN}	Microphone input impedance		40		kΩ
V_{MICIN}	Microphone input DC voltage		1.6		V
Amplifier					
GAIN	Overall gain (OUTP or OUTN) / MICIN According to I^2C settings	0		42	dB
DynOut	Output dynamic voltage swing (OUTP / OUTN)		1.8		Vpp
THD	Harmonic distortion on OUTP & OUTN 1 kHz, 1.8 V_{PP} output.			0.1	%
DCout	Output DC common voltage		1.6		V
R_{OUT}	Output impedance (OUTP / OUTN) I_{LOAD} < 300 µA		100		Ω
En	Input equivalent noise BW 20 Hz to 20 kHz / source impedance = 2.2kΩ		1.5		uVrms
PSR (diff)	Voltage supply rejection (diff: OUTP - OUTN) 42dB gain, +/-200mV ripple on AUD3v3 @ 1 kHz		40		dB
PSR (single)	Voltage supply rejection (OUTP / OUTN) 42dB gain, +/-200mV ripple on AUD3v3 @ 1 kHz		40		dB
LFc	Low cut-off frequency (C_{IN} = 2.2 µF)		20		Hz
HFc	High cut-off frequency		20		kHz

6.5 AC electrical characteristics

Table 22: Serial interface timing

Symbol	Parameter	Max.	Unit
f_{SCL}	SCL clock frequency	100	kHz

7 Optical Characteristics

7.1 Optical characterisation methods

The following measurements are made based on the pixel as summarized in *Table 23*.

Table 23: VV6501 Pixel overview

Parameter	Value	Unit
Size	5.6 x 5.6	µm
Architecture	3T, DDS	
Saturation voltage at pixel, V_{SAT} (Gain x1, 1024 codes)	1.2	V
FD capacitance	3.0	fF

Average sensitivity

The average sensitivity is a measure of the image sensor response to a given light stimulus. The optical stimulus is a white light source with a color temperature of 3200K, producing uniform illumination at the surface of the sensor package. For a color sensor, an IR blocking filter, CM500, is added to the light source. The analog gain of the sensor is set to x1. The exposure time, Δ**t**, is set as 50% of maximum. The illuminance, **I**, is adjusted so the average sensor output code, **Xlight**, is roughly mid-range equivalent to a saturation level of 50%. Once Xlight has been recorded the experiment is repeated with no illumination to give a value **Xdark.**

The sensitivity is then calculated as $\frac{Xlight - Xdark}{\Delta t \cdot I}$. The result is expressed in volts per lux-second.

Dark signal

The dark signal is a measure of the effect of pixel leakage current on the sensor output. The measurement is performed without illumination. As the dark signal is small the analog gain, **G**, of the sensor is increased to x4. For the same reason the clock divisor is set to16. As the leakage is highly temperature dependent, measurement is done at a controlled temperature of 25^{o}C. The mean sensor output is then recorded at 2 exposure settings: **Xdark** at the maximum exposure time; **Xblack** at zero exposure.

The dark signal is calculated as $\frac{Xdark - Xblack}{\Delta t \cdot G}$ and is expressed in volts per second.

Temporal noise of pixel and readout

A measure of the temporal noise is required to quantify the noise floor. As the signal is small the gain, **G**, is set to the maximum of x16. In order to remove fixed pattern noise sources it is calculated as the standard deviation, σ_{black}, of the difference of a pair of zero exposure and zero illumination images. Random noise is expressed in mV.

Dynamic range

The dynamic range is the measure of the maximum and minimum signal levels at which the sensor can be used.

The figure for temporal noise is used to find the dynamic range as follows $20 \cdot \log\left(\frac{G \cdot Vsat}{\sigma black}\right)$.

Sensor SNR

The SNR measurement given here is based on the temporal noise. The SNR is calculated as the pixel saturation voltage divided by the temporal noise at that saturation level. The optical setup is the same as for the measurement of average sensitivity. The sensor gain, **G**, is set to x1.

The SNR figure is then calculated as: $20 \cdot \log\left(\frac{G \cdot Vsat}{\sigma signal}\right)$.

Fixed Pattern Noise (FPN)

The FPN of an image sensor is the average pixel non-temporal noise divided by the average pixel voltage. The illumination source is the same as for the average sensitivity measurement. The FPN is calculated at coarse exposure settings of 0,10,150,250 and 302 with a gain set to 1. 10 frames are grabbed and averaged to produce a temporally independent frame before each calculation. FPN is expressed in mV.

Vertical Fixed Pattern Noise (VFPN)

VFPN describes the spatial noise in an image sensor related to patterns with a vertical orientation. The VFPN is defined as the standard deviation over all columns of the average pixel voltage for each column determined at zero exposure and zero illumination. VFPN is expressed in mV.

Shading

Shading describes how average pixel values per “block” change across the image sensor array. For fine shading calculations, the image sensor array is split into 30 pixel by 30 pixel blocks. An average value is then calculated for each block, averages are then compared across the whole device. The blocks are increased in size to 60 pixels by 60 pixels for the gross shading calculation. Shading is expressed in mV.

7.2 Optical characterisation results

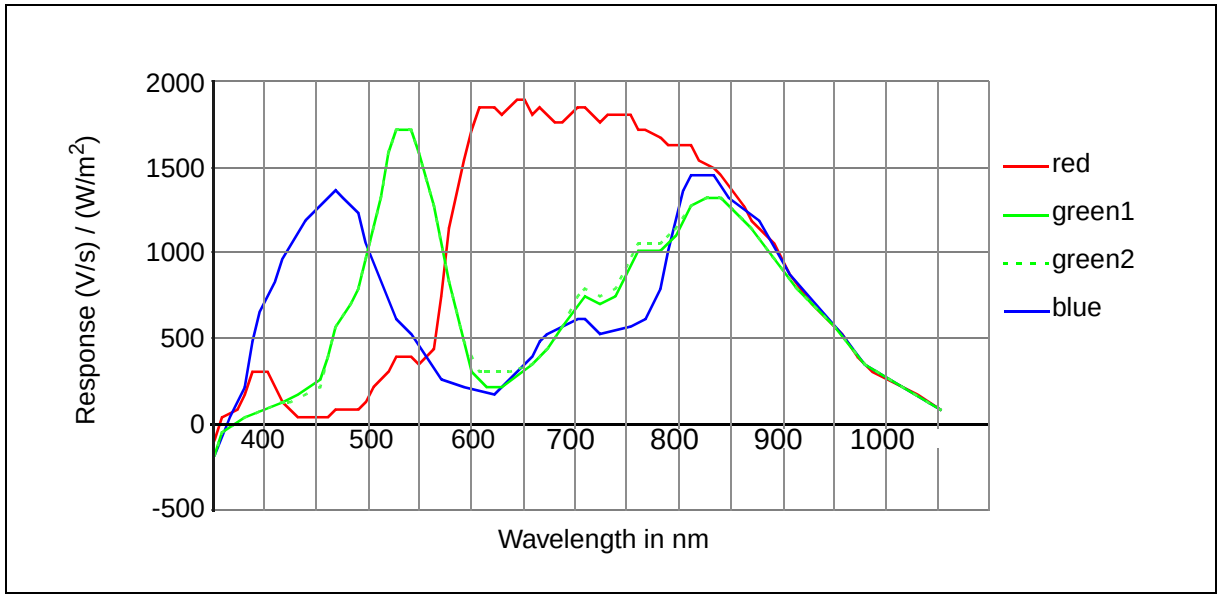
Table 24: Optical characterization

Optical parameter	Red	Green	Blue	Unit
Average sensitivity	-	2.05	-	V/lux.s
Dark signal	-	9.0	-	mV/s
Temporal noise	-	2.12	-	mV
Dynamic Range	-	54	-	dB
SNR	-	41	-	dB
Fixed Pattern Noise	-	1.13	-	mV
Vertical fixed pattern noise	-	0.68	-	mV
Shading (Gross)	1.1	1.3	1.0	%

7.3 Spectral response

The spectral response measurement is given below.

Figure 29: Spectral response



7.4 Blooming

We do not perform any test measurements for blooming.

Blooming is a phenomenon that does not affect CMOS sensors the same way as CCD imagers are afflicted. CCD blooming can cause an entire column or set of columns to flood and saturate.

8 Defect Categorisation

8.1 Introduction

Two distinct categories of defects are discussed in this section:

- Pixel defects (*Section 8.2* - *Section 8.5*)
- Physical aberrations (*Section 8.6*)

The two categories differ in terms of test methodology as explained below.

8.2 Pixel defects

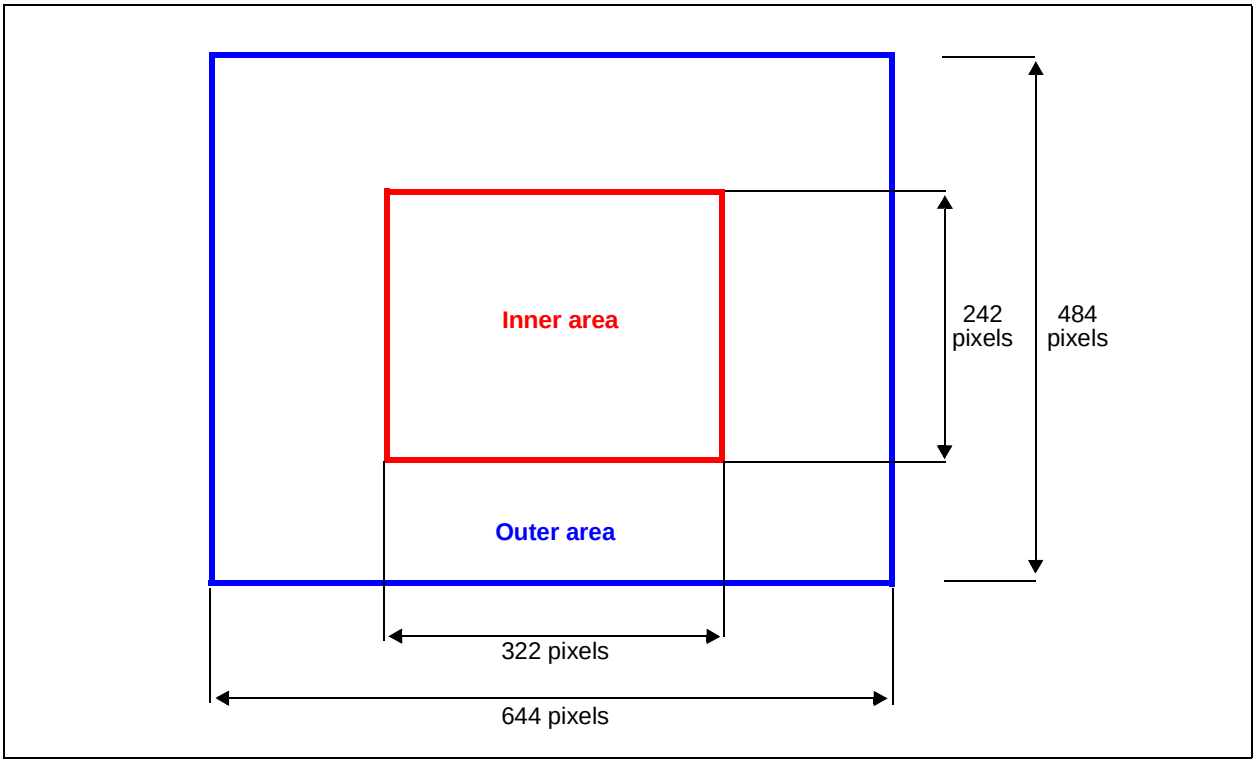
All packaged CMOS image sensors can contain impurities, either silicon faults, optical blemishes or external dirt particles which can be introduced in the product at various stages of the manufacturing process. These impurities can result in pixel defects, that is a pixel whose output is not consistent with the level of incident light falling on the image sensor. Precise definitions of the type of pixel defect tested by STMicroelectronics are outlined below. The ability to identify and correct these defects is central to both the design requirements and quality certification, via test of STMicroelectronics sensor products.

STMicroelectronics produces a number of hardware co-processors and software drivers that implement defect correction algorithms. The defect correction algorithms ensure that the VV6501 sensor in conjunction with a companion STMicroelectronics co-processor will produce a high quality final image.

8.3 Sensor array area definition

For specific aspects (refer to couplet test, see *Section 8.4.3*) of pixel defect testing, the image sensor array is subdivided into two regions as follows:

Figure 30: VV6501 array



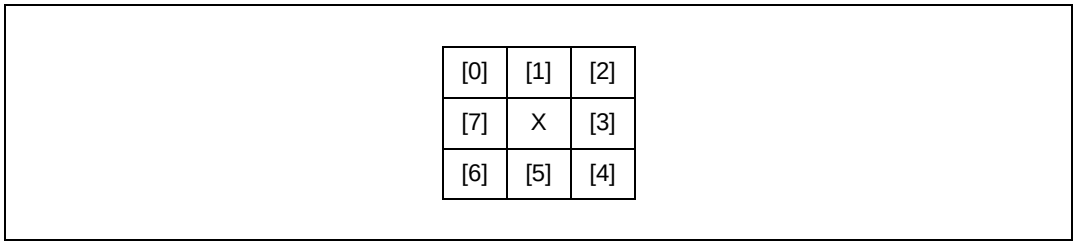
The inner array in *Figure 30* above is centre justified, in the x and y axis, with respect to the outer array. The inner array is 50% of the full width and 50% of the full height of the larger outer array, therefore the inner array is one quarter of the area of the outer array.

8.4 Pixel fault definitions

8.4.1 Pixel fault numbering convention

Please find the pixel notation described in *Figure 31* below. For test purpose, the 3x3 array describes 9 Bayer pixels of a common color, that is all the pixels will either be Red, Green or Blue. The pixel under test is **X**.

Figure 31: Pixel numbering notation

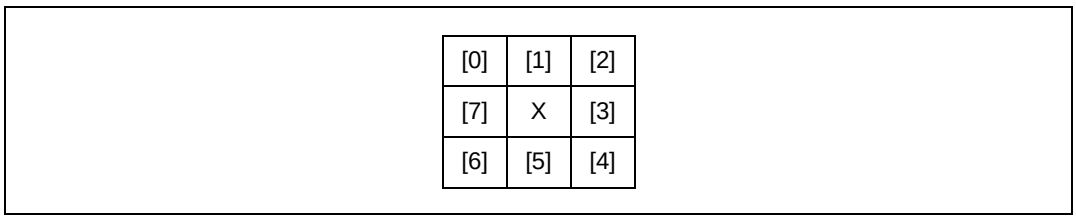


8.4.2 Single pixel faults

STMicroelectronics define a single pixel fail as a failing pixel with no adjacent failing neighbors of the same colour. A single pixel fail can be a “stuck at white” where the output of the pixel is permanently saturated regardless of the level of incident light and exposure level, a “stuck at black” where the pixel output is zero regardless of the level of incident light and exposure level or simply a pixel that differs from its immediate neighbors by more than the test threshold, that is differ by more than 8.0% from pixel average of color space neighbors.

In the example below in *Figure 32*, we assume that the pixel ‘X’ is a fail. This pixel is qualified as single pixel fail if the pixels at positions [0],[1],[2],[3],[4],[5],[6] and [7] are “good” pixels that pass the final test. The implemented test program qualifies a sensor with up to 120 single pixel faults. Defect correction algorithms correct the single pixel faults in the final image.

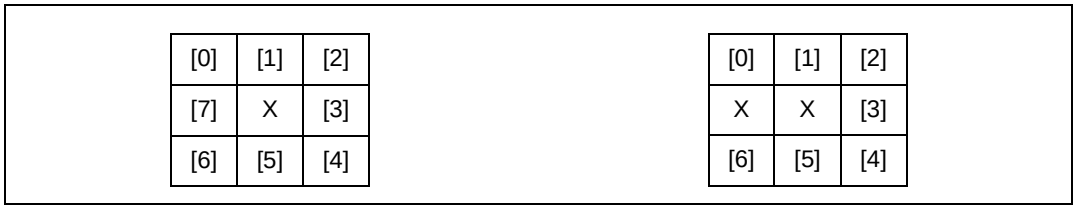
Figure 32: Single pixel fault



8.4.3 Couplet definition

A failing pixel at **X** with a failing pixel at position [0] or [1] or [2] or [3] or [4] or [5] or [6] or [7] such that there is a maximum of 2 failing pixels from the group of 9 pixels illustrated in *Figure 33* is described as a couplet fail. The example shown on the right in *Figure 33* has failing pixels at the centre location and at position [7].

Figure 33: General couplet examples



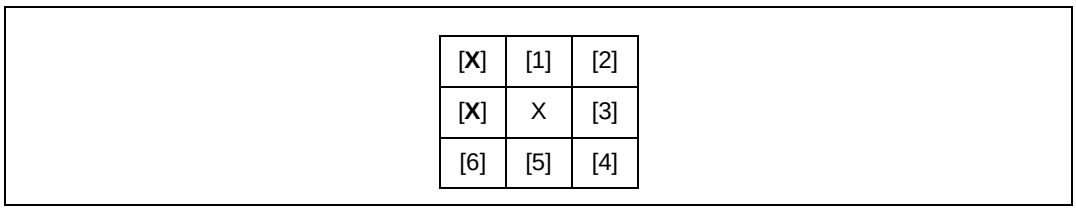
The basic couplet definition is further subdivided into minor and major couplets. With respect to the example in *Figure 33*, a minor couplet is defined as a defect pixel pair where one pixel can be an extreme fail, that is a “stuck at black” or “stuck at white”, but the second pixel in the pair must differ from the local pixel average by less than 15% of that average value. If the second pixel in the couplet differs by more than 15% of the local pixel average value then this would be defined as a major couplet.

Note that the test program considers a couplet as 2 independent pixels. If the test identifies two independent pixel fails (pixels that differ by more than 15% from pixel average of neighbors) that form a couplet with 2 minor pixel fails within the inner area, the device fails the test and is rejected. If however the test identifies 2 couplets where the pixels span the border between the inner and outer areas and where only one of the pixels in the inner area is determined as a major fail and the other a minor fail, then this device passes the test.

8.4.4 Cluster definition

We define a cluster fail as a failing pixel with at least two adjacent failing pixels. In the example from *Figure 34*, there are additional pixel fails in positions [0] and [7]. This example constitutes a cluster. A sensor containing a cluster is always rejected.

Figure 34: Cluster example



8.5 Summary pass criteria

Table 25: Sensor pixel defect pass criteria

Single pixel fails	Minor Couplet[a]	Major Couplet[b]	Clusters
<=120	1 (2)	0	0

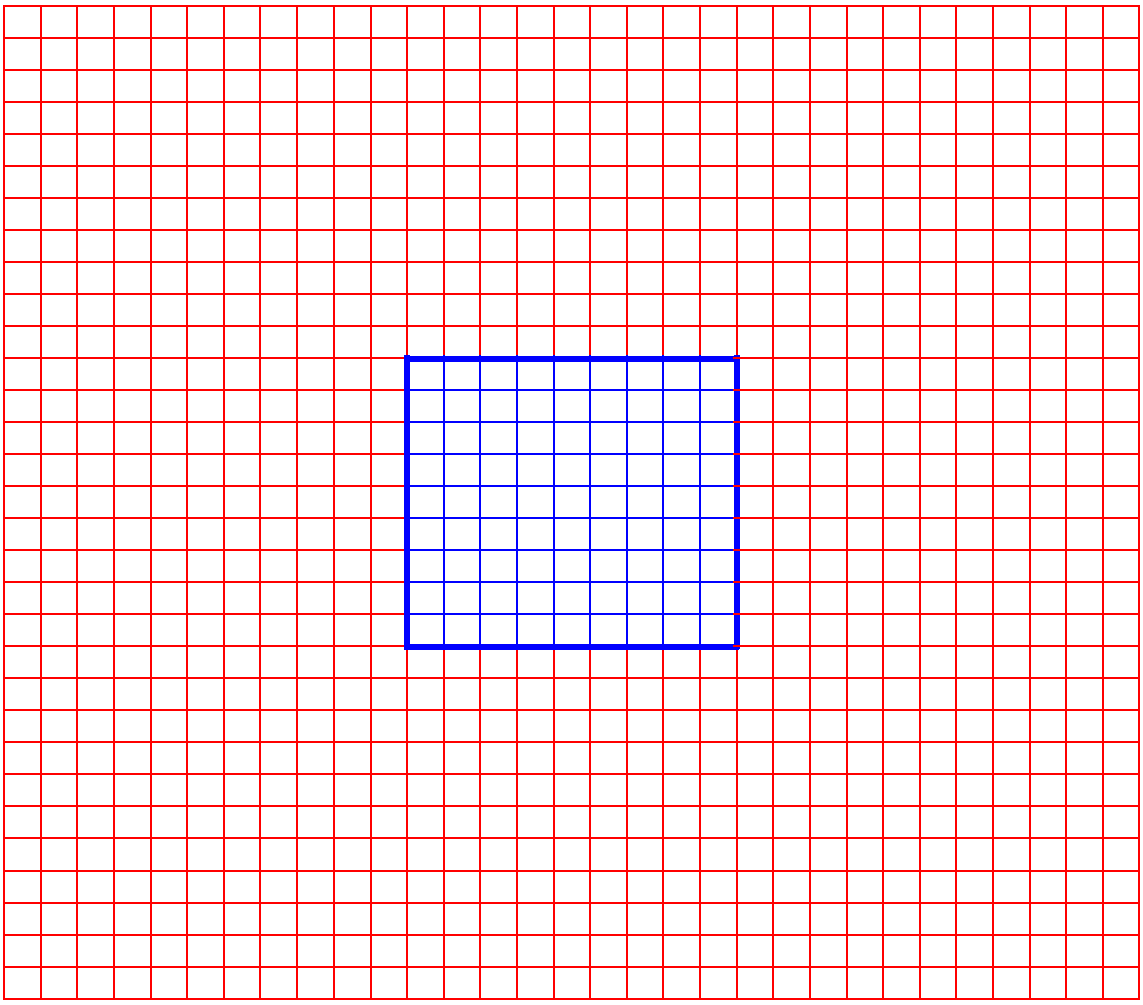
a. Test program will allow maximum of one minor couplet in inner zone of pixel array.
Test program will allow maximum of two minor couplets in outer zone of pixel array.
b. No major couplet allowed.

8.6 Physical aberrations

Silicon surface irregularities and external marks, both pits and deposits, on the package glass lids can cause a deterioration in image quality. STMicroelectronics recognize that this could compromise the product quality and therefore have introduced a specific test algorithm to identify and reject samples that display these phenomena. The pass/fail criteria for this test are given in *Section 8.6.1*.

8.6.1 Test details

Figure 35: Test area definition



The test defines 2 areas:

- A small area: 9 by 9 pixels with pixel under test at the centre of this area (shaded blue in *Figure 35*)
- A large region, 31 by 31 pixels (shaded red in *Figure 35*)

An average value is calculated for both the ‘small’ and ‘large’ areas.The areas then scan across the whole array so that every pixel is evaluated. Due to the nature of the test, only the red pixels are used. The next stage of the test is the creation of a pixel map with the coordinates of the failing pixels. A pixel location is identified as a fail in the map if it satisfies the criteria outlined in *Table 26* below.

Table 26: Criteria for pixel to be entered in failure map

Pixel location is a fail in map if
Small average < Large average - (1.2% of Large average) or Small average > Large average + (1.2% of Large average)

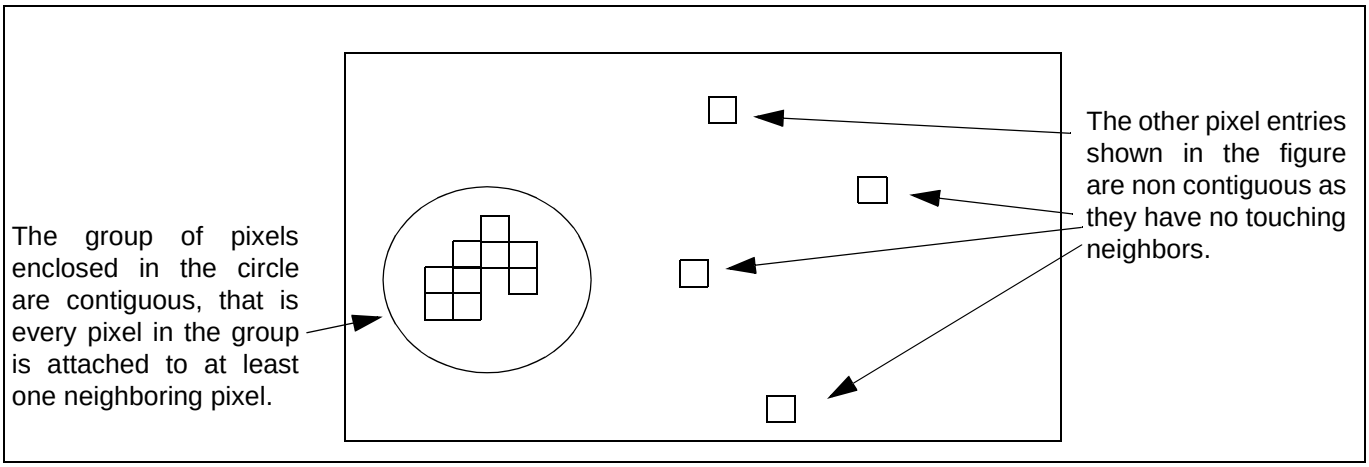
The contents of the fail map determine whether the sensor fails the physical aberration test. The fail criteria are given in *Table 27* below:

Table 27: Physical aberration test fail criteria

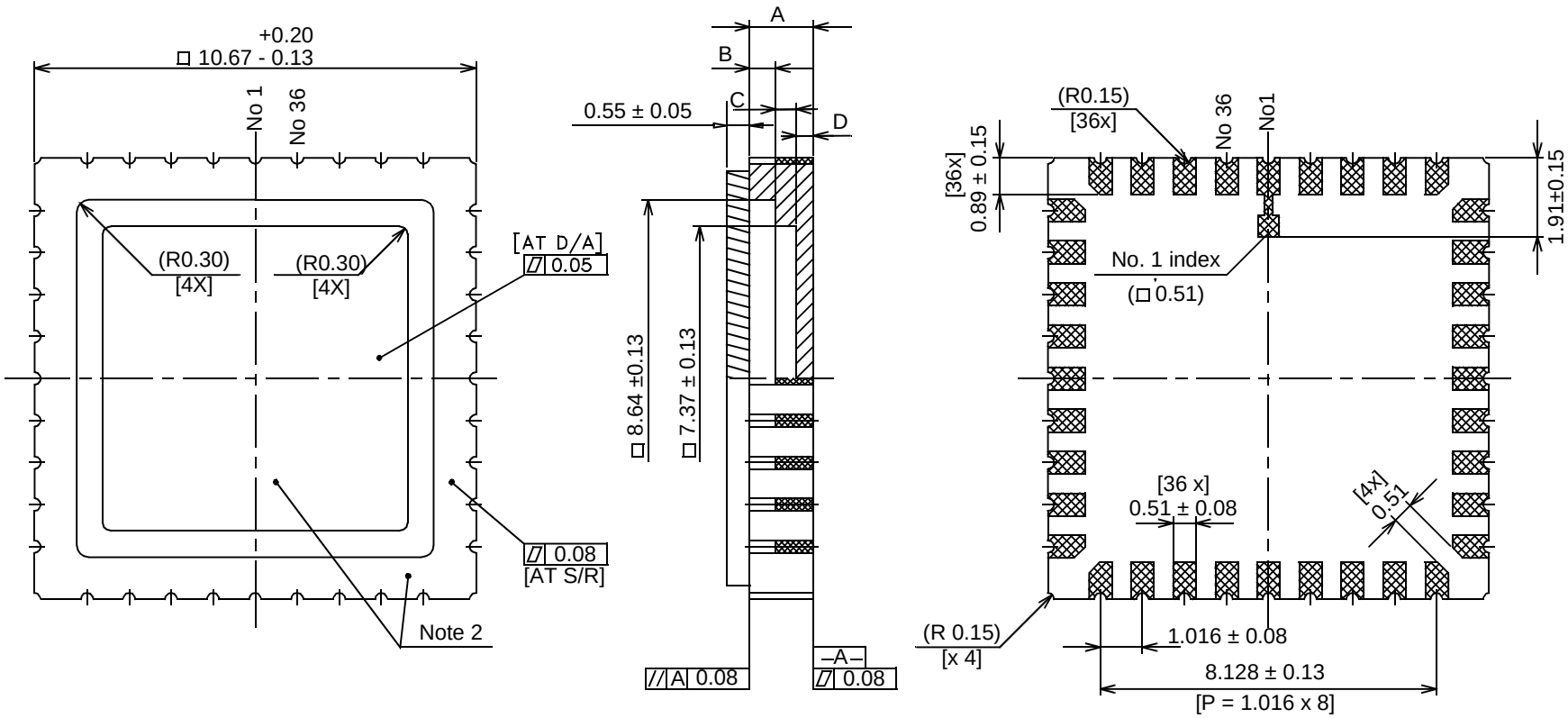
Fail physical aberration test if
> 82 contiguous[a] pixel entries in the failure map

a. An example of contiguous pixels entries is given in *Figure 36*

Figure 36: Contiguous pixels example



9 Package Mechanical Data



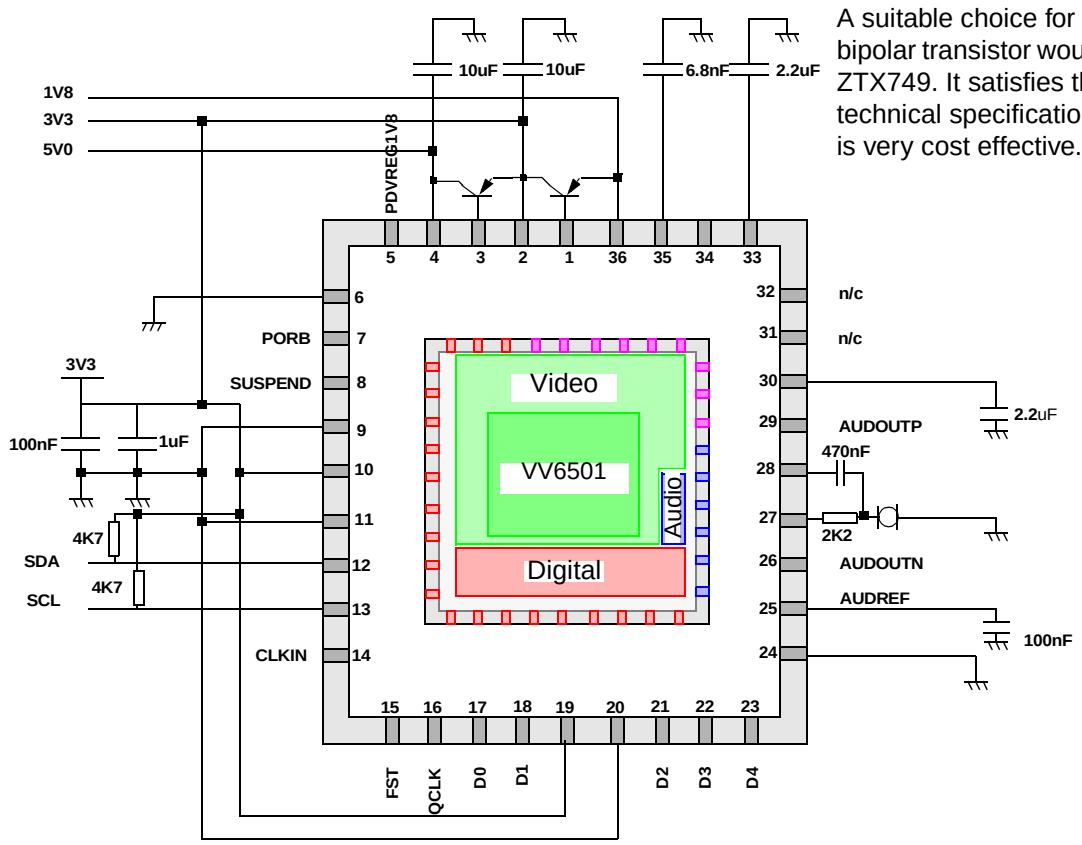
Notes:
1. Gold plate 0.3 µm minimum over 1.27 ~ 8.89 µm nickel
2. Seal area and die attach area shall not be without metallization
3. All tolerances are ±0.13 unless otherwise specified

	Option K	Option N
A	1.549 ± 0.161	1.54 ± 0.16
B	0.571 ± 0.05	(0.62)
C	0.546 ± 0.05	0.51± 0.05
D	0.432 ± 0.05	0.41 ± 0.03

10 Design-In Information

10.1 Basic support circuit

Figure 37 : Basic support circuit



STMicroelectronics advises the use of a grounding star point. All decoupling capacitors should be placed as close to sensor as possible.
The support circuit outlined above describes a USB based system with a nominal 5V supplying the device.

10.2 Transistor choice

The ZTX749 has a high min. H_{FE} (lower on-chip current). It is also inexpensive and has good heat dissipation.

10.3 Pin 1 and image orientation

Please note that for the sensor array to produce a correctly aligned image, pin 1 should be located at the ‘top’ rather than 180 degrees rotated at the ‘bottom’ (see *Figure 3*).

11 Evaluation Kits

Evaluation kits are available to demonstrate the VV6501 sensor technology.

The sensor can be demonstrated using the PCI card based standard evaluation kit STV-EVK-E01. A daughter card kit is also available to purchase separately. The daughter card is a simple pcb on which the sensor is mounted. The daughter card can then be plugged into the main evaluation kit pcb.

The evaluation kit is supplied with supporting software that enables the customer to program the sensor via an I^2C interface.

Table 28: Ordering details

Part Number	Description
STV-EVK-E01	Sensor only evaluation kit for VV6501C001
STV-6501C-D01	Sensor daughter card for VV6501C001